Voltage unbalance compensation of Flying Capacitor based on a dynamic Pulse Width Modulation applied to a Flying Capacitor leg inverter

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Mariem Jday · **Paul-Etienne Vidal**

Abstract This paper introduces a dynamic Pulse Width Modulation scheme, apply to *N*-level Flying Capacitor inverter. A mathematical approach is detailed to solve the expression of a linear system that model the inverter leg considered. Some degrees of freedom, that have to be set, are exhibited. The proposed technique relies on the relationship made between the degrees of freedom and the voltage unbalance of the floating capacitors. Simulation results are provided to illustrate the performance of such a modulation scheme.

1 Introduction

Static power converters controlled by Pulse Width Modulation (PWM) are frequently used in various industrial applications such as power generation systems [1], energy transportation systems, etc. In order to improve the overall performance of these applications, multilevel converters, a particular class of converters, are now used in a wide range of industry applications [2]. Effectively, the use of two-level power converters in high-voltage applications causes an increase of the blocking voltage of semiconductors. The use of multilevel converter structure can mitigate this problem. Several multilevel architectures have emerged in the last three decades [3]. Among them, the Flying Capacitor inverter (FC inverter) is defined [4]. This converter has intermediate voltage sources formed by floating capacitors. This converter requires balanced voltages for every floating capacitors. This functioning constraint generates a great interest to ensure the floating capacitor voltage balanced, thanks to the control applied to the converter [5].

It has been demonstrated that, in the absence of any fault, the usual carrier based PWM control ensures the natural balance of the capacitor voltages. Several studies have been made on the control of multicell series converters in order to increase the performance of the converter. A particular technique, the Space Vector Pulse Width Modulation scheme (SVPWM), was presented to achieve the best performance. SVPWM consists of monitoring the output voltage as a rotating vector, and representing it on a diagram, following the states of switches. Nevertheless, for large system, SVPWM is difficult to design.

In recent years, a generic model of PWM Voltage Source Inverter (VSI) was proposed [6], [7]. It is based on a generic and average model of the three-phase converter. This generic model allows to describe the inner topology of every leg and, by the use of several mathematical tools, to generate the relationships between duty cycles to apply, and the desired average output voltages. As a matter of facts, the method finally helps generating the PWM scheme to apply, whatever the topology or the number of level desired. During the process to express the duty cycles, some degrees of freedom, that have to be set, are generally exhibited.

In this work, the aim is to use the generic framework described previously to ensure floating capacitor voltage balance, thanks to the PWM scheme. A PWM scheme that allows to exploit the measured or estimated capacitor voltages will be used. The floating capacitor voltage measurement will be finally related to the degrees of freedom. Indeed, every duty cycle generated will ensure voltage balance and low harmonic output current.

This paper is made of five parts. In the second section, an average model of N-level FC inverter is described. A PWM control strategy is deduced. In third and fourth sections, the previous model is applied to a 3 level and 5 level FC inverter, respectively. In the fifth section, and for the latter

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topology, the number of degrees of freedom, their ranges of use and their expressions, are determined. This section ends with simulations performed on Matlab/Simulink. Simulations show the performance and robustness of the proposed control strategy, compared to the usual PWM control. More precisely, the robustness is assessed when a fault produces a floating capacitor unbalance.

2 N-level generic PWM scheme for Flying Capacitor topology

2.1 PWM Flying Capacitor model

N is the number of level that can be reached by the output voltage v_{ao}. The N-level FC is composed of nested elementary switching cells, with per level capacitor as illustrated by figure 1. $p = N - i$, stands for the ratio value of the voltage source E applied to the capacitor C_i of the switching cell i.

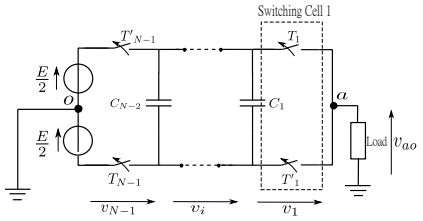

Fig. 1 Isolated leg of a N-level FC inverter.

The elementary switching cell numbered i, is made of T_i and its complementary switch $T_i^{'}$, and the floating capacitor C_i. When $T_i = 1$, the switch is ON, OFF elsewhere. Within the inner FC structure, the difference between the two capacitors' voltage is $\dfrac{E}{N-1}$. For the leg connected to a load at point a, the line voltage v_{ao} is

$$v_{ao} = \sum_{i=1}^{N-1} v_i - \frac{E}{2}\,, \tag{1}$$

where v_i, is the lower switch T_i' voltage as illustrated in Fig. 2.

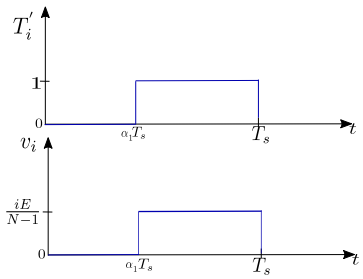

Fig. 2 Voltage waveform v_i of an isolated switch T_i'.

The switching frequency f_s is at least ten times greater than the load steady state frequency f_0. In this functioning, the switch voltage v_i is assimilated to its average value during T_s. The average voltage is denoted V_i and is expressed as

$$< v_i >_{T_s} = V_i = \frac{1}{T_s}\int_0^{T_s} v_i dt = \frac{E}{N-1}\alpha_i\,, \tag{2}$$

where α_i is the duty cycle applied to the switching cell i. More precisely α_i is the time ratio when T_i is turned on over the switching time T_s. For every switching cell of the leg, the duty cycle column vector α is defined such as

$$\alpha = \left[\alpha_1 \ \ldots \ \alpha_i \ \ldots \ \alpha_{(N-1)}\right]^T. \tag{3}$$

Then, using equations (1) and (2), a $(1\times(N-1))$ matrix S_{FC} is defined such as $S_{FC} = \left[\frac{1}{N-1} \ \ldots \ \frac{1}{N-1}\right]$. Obviously, this relationship can be extended to every supplementary phase. Indeed, the average output voltage applied to the load V_{ao}^* is

$$V_{ao}^* = < v_{ao} >_{T_s} + \frac{E}{2} = E\,S_{FC}\,\alpha\,. \tag{4}$$

2.2 Solution set

The duty cycles are expressed such as [6],

$$\alpha = \frac{1}{E}S_{FC}^{\dagger}V_{ao_{ref}}^* + \left(I_{(N-1)\times(N-1)} - S_{FC}^{\dagger}S_{FC}\right)z\,, \tag{5}$$

where $S_{FC}^{\dagger}$ is the pseudo-inverse of S_{FC}. z is an arbitrary column vector that allows to explore the solution set according to the physical constraints for α. Equation (5) can be defined as the sum of fixed part α_f and a variable part α_v:

$$\alpha = \alpha_f + \alpha_v\,, \text{such as} \quad \begin{cases} \alpha_f = \dfrac{1}{E}S_{FC}^{\dagger}V_{ao_{ref}}^* \\ \alpha_v = \left(I_{(N-1)\times(N-1)} - S_{FC}^{\dagger}S_{FC}\right)z \end{cases} \tag{6}$$

The Sylvester theorem states that the number of degrees of freedom (d.o.f), is linked to the size of the kernel of S_{FC} such as,

$$n_{\text{d.o.f.}} = dim\left(ker\left(S_{FC}\right)\right)\,. \tag{7}$$

In the following, the variable part will be linked to d.o.f expression. The linear system described in Eq. (4) is consistent, and admits an infinity of solution. Indeed,

$$\begin{cases} rank(S_{FC}) & = rank([S_{FC} \quad V_{ao}^*]) \\ rank(S_{FC}) & < \text{Number of row of } V_{ao}^*\,. \end{cases} \tag{8}$$

Effectively, as $rank(S_{FC}) = 1$, S_{FC} is singular and its pseudo inverse is obtained easily. If applied to a N-level inverter, the equation (7) is expressed as

$$n_{d.o.f.} = \text{Number of row of } (S_{FC}) - rank(S_{FC}) = N - 2 \tag{9}$$

The d.o.f are expressed as a column vector denoted λ, by the mean of the maximal rank factorization. Firstly, the several d.o.f. are grouped into λ such as

$$\lambda = \left[\lambda_1, \ldots, \lambda_{n_{d.o.f.}}\right]^T. \tag{10}$$

Secondly, two matrices, $F_{((N-1)\times(N-2))}$ and $G_{((N-2)\times(N-1))}$, are chosen such as

$$\left(I_{(N-1)} - S_{FC}^{\dagger} S_{FC}\right) = FG. \tag{11}$$

Then, assuming $Gz = \lambda$, the solution is

$$\alpha = \frac{1}{E}(S_{FC}^{\dagger}) V_{ao_{ref}}^{*} + F\lambda. \tag{12}$$

As a matter of facts, the fixed solution α_f is :

$$\alpha_f = \frac{1}{E} S_{FC}^{\dagger} V_{ao_{ref}}^{*}; \tag{13}$$

and the variable part α_v:

$$\alpha_v = F\lambda. \tag{14}$$

2.3 Boundaries expression for the solution set

One advantage of the generic model expressed previously, is to establish the d.o.f boundaries to get admissible solutions. More precisely, as the modeling process is based on intersective modulation assumption, it implies that every duty cycle α_i is such as:

$$0 \leq \alpha_i \leq 1. \tag{15}$$

As a matter of fact, it leads to express every variable part α_{v_i} separately. Obviously F has to be known:

$$-\alpha_f \leq \alpha_v \leq 1 - \alpha_f \Leftrightarrow -\alpha_f \leq F\lambda \leq 1 - \alpha_f, \tag{16}$$

assuming that the fixed part α_{f_i} is known. Indeed, the final choice for λ_i is done following Eq. (16) and some additional criteria such as switching losses or Total Harmonic Distortion (THD), that will be discussed in the following sections. In the following, the application of the generic model to 3-level and 5-level FC converters will be done.

3 Average model of 3-level FC inverter

Figure 3 presents the structure of a 3-level FC inverter, where v_1 and v_2 are the the elementary voltages. The average voltages' values are expressed as:

$$V_1 = \frac{E}{2}\alpha_1, \qquad \text{and} \qquad V_2 = \frac{E}{2}\alpha_2. \tag{17}$$

Moreover, the output voltage v_{ao} is:

$$v_{ao} = v_1 + v_2 - \frac{E}{2}. \tag{18}$$

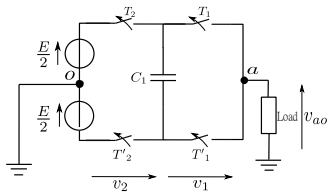

Fig. 3 Isolated leg of a 3-level FC inverter

Using expression (4), the average output voltage applied to the load V_{ao}^{*} is

$$V_{ao}^{*} = < v_{ao} >_{T_s} + \frac{E}{2} = E\, S_{FC}\, \alpha, \tag{19}$$

such as $S_{FC} = \left[\frac{1}{2}\ \frac{1}{2}\right]$ and $\alpha = \left[\alpha_1\ \alpha_2\right]^T$. Consequently, α is given as:

$$\alpha = \frac{1}{E} S_{FC}^{\dagger} V_{ao_{ref}}^{*} + \left(I_{2\times 2} - S_{FC}^{\dagger} S_{FC}\right) z, \tag{20}$$

where $S_{FC} = \left[\frac{1}{2}\ \frac{1}{2}\right]$ and $S_{FC}^{\dagger} = \left[1\ 1\right]^T$. The fixed and variable parts of α are deduced such as:

$$\alpha_f = \frac{1}{E}\left[1\ 1\right]^T V_{ao_{ref}}^{*} \tag{21}$$

$$\alpha_v = \left(I_{2\times 2} - S_{FC}^{\dagger} S_{FC}\right) z. \tag{22}$$

As the number of row of $(S_{FC}) - rank(S_{FC}) = 1$, it exists 1 degree of freedom. Indeed, the α_v is expressed as $\alpha_v = F\ \lambda$, where F is a matrix obtained by the full rank factorisation of $\left(I_{2\times 2} - S_{FC}^{\dagger} S_{FC}\right) z$.

Finally, F is computed as $F = \left[\frac{-1}{\sqrt{2}}\ \frac{1}{\sqrt{2}}\right]^T$. Indeed, the solution α is expressed:

$$\alpha = \frac{1}{E}\begin{bmatrix}1\\1\end{bmatrix} V_{ao_{ref}}^{*} + \begin{bmatrix}\frac{-1}{\sqrt{2}}\\ \frac{1}{\sqrt{2}}\end{bmatrix} \lambda. \tag{23}$$

In order to find out the full expression of α, the degree of freedom λ must be fixed. However, the boundaries for λ must be first defined, to ensure that the duty cycles evolves in the interval $[0,1]$. Using expression (23), and (16), the margin of λ are such as

$$\begin{cases} max(\frac{\sqrt{2}}{E} V_{ao_{ref}}^{*} - \sqrt{2}), (\frac{-\sqrt{2}}{E} V_{ao_{ref}}^{*})) \leq \lambda \\ \lambda \leq min(\frac{\sqrt{2}}{E} V_{ao_{ref}}^{*}, \sqrt{2} - \frac{\sqrt{2}}{E} V_{ao_{ref}}^{*}) \end{cases}. \tag{24}$$

More details will be presented in the next section to illustrate the relationship of the capacitor voltage and the degree of freedom λ.

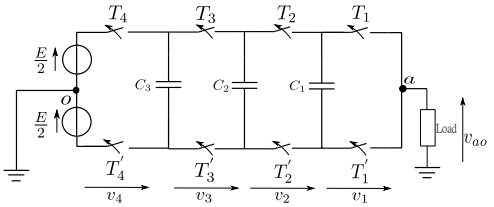

Fig. 4 Isolated leg of a 5-level FC inverter.

4 Average model of 5-level FC inverter

Figure 4 presents a 5-level FC inverter. v_1, v_2, v_3 and v_4 are the elementary voltages of each cell of the inverter. The average output voltage V^*_{ao} is

$$V^*_{ao} = V_1 + V_2 + V_3 + V_4 = E\ S_{FC}\ V^*_{ao_{ref}}, \tag{25}$$

where $S_{FC} = \left[\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\right]$. Then, every $\left[\alpha_1\ \alpha_2\ \alpha_3\ \alpha_4\right]^T$ is split in a fixed solution α_{f_i} and a variable one α_{v_i}, that are expressed using expression (6). As number of row of $(S_{FC}) - rank(S_{FC}) = 3$, there is 3 degrees of freedom, $n_{d.o.f.} = 3$. The use of the maximal rank factorisation allows to establish α_v as follows:

$$\alpha_v = \begin{bmatrix} -\frac{3}{2\sqrt{3}} & 0 & 0 \\ \frac{1}{2\sqrt{3}} & -\frac{2}{\sqrt{6}} & 0 \\ \frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} \\ \frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3, \end{bmatrix}. \tag{26}$$

The final expression of α is deduced as

$$\begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \end{bmatrix} = \frac{1}{E} \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} V^*_{ao_{ref}} + \begin{bmatrix} -\frac{3}{2\sqrt{3}} & 0 & 0 \\ \frac{1}{2\sqrt{3}} & -\frac{2}{\sqrt{6}} & 0 \\ \frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} \\ \frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3, \end{bmatrix}. \tag{27}$$

5 Margins of the degrees of freedom λ

Based on the expression given in expression (24), the margins of each λ are detailed in the following.

5.1 Margins of λ_1

Note that all α_i depends on λ_1. Therefore, it is possible to use first a single equations of α_i to define the margins of λ_1.

$$\alpha_1 = \frac{V^*_{ao_{ref}}}{E} - \frac{3}{2\sqrt{3}}\lambda_1\,. \tag{28}$$

The first margins of λ_1 is defined using the condition $0 \leq \alpha_1 \leq 1$ which leads to set :

$$\frac{2\sqrt{3}}{3}\left(\frac{V^*_{ao_{ref}}}{E} - 1\right) \leq \lambda_1 \leq \frac{2\sqrt{3}V^*_{ao_{ref}}}{3E} \tag{29}$$

Secondly, in order to find a suitable correlation between α_4, α_3, α_2 and λ_1, the following equality is used:

$$\alpha_2 + \alpha_3 + \alpha_4 = \frac{3V^*_{ao_{ref}}}{E} + \frac{3}{2\sqrt{3}}\lambda_1. \tag{30}$$

Hence, there exists a second margin for λ_1:

$$-2\sqrt{3}\frac{V^*_{ao_{ref}}}{E} \leq \lambda_1 \leq 2\sqrt{3}\left(1 - \frac{V^*_{ao_{ref}}}{E}\right) \tag{31}$$

Finally, the overall boundaries of λ_1 are expressed as follows:

$$\begin{cases} \max\left(-2\sqrt{3}\frac{V^*_{ao_{ref}}}{E}, \frac{2\sqrt{3}}{3}\left(\frac{V^*_{ao_{ref}}}{E} - 1\right)\right) \leq \lambda_1 \leq \\ \min\left(2\sqrt{3}\left(1 - \frac{V^*_{ao_{ref}}}{E}\right), \frac{2\sqrt{3}V^*_{ao_{ref}}}{3E}\right) \end{cases} \tag{32}$$

5.2 Margins of λ_2

Based on the duty cycle equations, it is noticed that α_2, α_3 and α_4 depends on λ_2. Since $0 \leq \alpha_2 \leq 1$ and $0 \leq \alpha_3 + \alpha_4 \leq 2$, the overall boundary of λ_2 is expressed such as $\lambda_{2_{min}} \leq \lambda_2 \leq \lambda_{2_{max}}$:

$$\begin{cases} \lambda_{2_{min}} = \\ \max\left(\frac{\sqrt{6}}{2}\left(\frac{V^*_{ao_{ref}}}{E} + \frac{\lambda_1}{2\sqrt{3}} - 1\right), \sqrt{6}\left(-\frac{V^*_{ao_{ref}}}{E} - \frac{\lambda_1}{2\sqrt{3}} - 1\right)\right) \\ \lambda_{2_{max}} = \\ \min\left(\frac{\sqrt{6}}{2}\left(\frac{V^*_{ao_{ref}}}{E} + \frac{\lambda_1}{2\sqrt{3}}\right), \sqrt{6}\left(1 - \frac{V^*_{ao_{ref}}}{E} - \frac{\lambda_1}{2\sqrt{3}}\right)\right) \end{cases} \tag{33}$$

5.3 Margins of λ_3

Similarly, given that $0 \leq \alpha_3 \leq 1$ and $0 \leq \alpha_4 \leq 1$, the overall margin for λ_3 are defined such as, $\lambda_{3_{min}} \leq \lambda_3 \leq \lambda_{3_{max}}$:

$$\begin{cases} \lambda_{3_{min}} = \\ \max\left(\frac{2}{\sqrt{2}}\left(\frac{V^*_{ao_{ref}}}{E} + \frac{\lambda_1}{2\sqrt{3}} + \frac{\lambda_2}{\sqrt{6}} - 1\right), \right. \\ \qquad \left. \frac{2}{\sqrt{2}}\left(-\frac{V^*_{ao_{ref}}}{E} - \frac{\lambda_1}{2\sqrt{3}} - \frac{\lambda_2}{\sqrt{6}}\right)\right) \\ \lambda_{3_{max}} = \\ \min\left(\frac{2}{\sqrt{2}}\left(\frac{V^*_{ao_{ref}}}{E} + \frac{\lambda_1}{2\sqrt{3}} + \frac{\lambda_2}{\sqrt{6}}\right), \right. \\ \qquad \left. \frac{2}{\sqrt{2}}\left(-\frac{V^*_{ao_{ref}}}{E} - \frac{\lambda_1}{2\sqrt{3}} - \frac{\lambda_2}{\sqrt{6}} + 1\right)\right) \end{cases} \tag{34}$$

5.4 Influence of the d.o.f on dynamic behaviour of floating capacitor voltages

The current i_{Ci} of the capacitor C_i is expressed as:

$$i_{Ci} = C_i \frac{dv_{Ci}}{dt}, \tag{35}$$

where v_{Ci} is the voltage across the capacitor C_i. One the one hand, the expression (35), integrated onto the switching period T_s is equivalent to:

$$T_s I_{ch}(\alpha_{i+1} - \alpha_i) = C_i \Delta v_{Ci} \tag{36}$$

On the other hand, expression (27) leads to the following equations:

$$\begin{cases} \alpha_4 - \alpha_3 = \sqrt{2}\lambda_3 \\ \alpha_3 - \alpha_2 = \frac{3}{\sqrt{6}}\lambda_2 - \frac{1}{\sqrt{2}}\lambda_3 \\ \alpha_2 - \alpha_1 = \frac{2}{\sqrt{3}}\lambda_1 - \frac{2}{\sqrt{6}}\lambda_2 \end{cases} \tag{37}$$

Finally base on expression (36), the 3 λ_i allows to be compute dynamically before the carrier based comparison stage:

$$\begin{cases} \lambda_3 = \frac{C_3 \Delta v_{C3}}{\sqrt{2} T_s I_L} \\ \lambda_2 = \frac{C_3 \Delta v_{C3} \sqrt{6}}{6 T_s I_L} + \frac{C_2 \sqrt{6} \Delta v_{C2}}{3 T_s I_L} \\ \lambda_1 = \frac{C_3 \Delta v_{C3}}{2\sqrt{3} T_s I_L} + \frac{C_2 \Delta v_{C2}}{\sqrt{3} T_s I_L} + \frac{C_1 \sqrt{3} \Delta v_{C1}}{2 T_s I_L} \end{cases} \tag{38}$$

One notes that Δv_{Ci} is the sweeping of the voltage v_{Ci} during a period T_s such as:

$$\forall t, \Delta v_{Cj}(t) = v_{Cj_{ref}} - v_{Cj_{mes}}, \tag{39}$$

where $v_{Ci_{ref}}$ is the reference voltage value of v_{Ci}, $v_{Ci_{mes}}$ and I_L are the C_i voltages and load current measurements, respectively.

5.5 Simulation

A simulation on Matlab/Simulink is performed. The simulation is based on the 5-level inverter described in section 4 and Figure 4. The parameters used are depicted in Tab. 1. Firstly, the duty cycles are generated using the method presented in the previous sections. Secondly, a carrier based scheme is applied, with two $\frac{\pi}{2}$ shifted triangular carriers, varying from 0 to 1 @f_s.

Table 1 Simulation parameters

Parameter	Value
DC source E	230 V
Load steady state frequency f_0	50 Hz
Switching frequency f_s	10 kHz
Capacity C_i	40 μF
Resistance R_1	100 Ω
Load resistance R	10 Ω
Load inductance L	1 mH

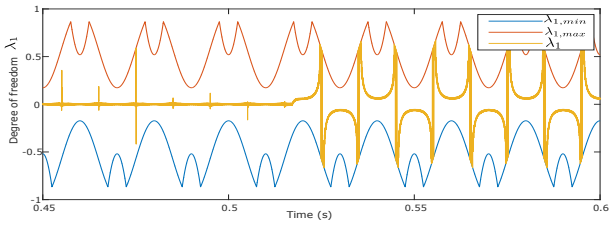

Fig. 5 Degree of freedom λ_1

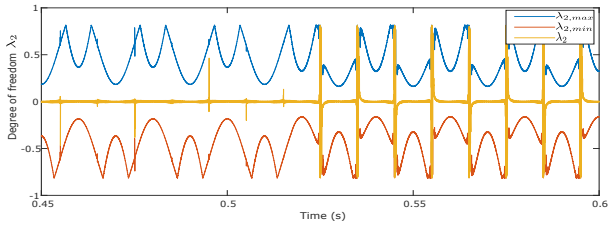

Fig. 6 Degree of freedom λ_2

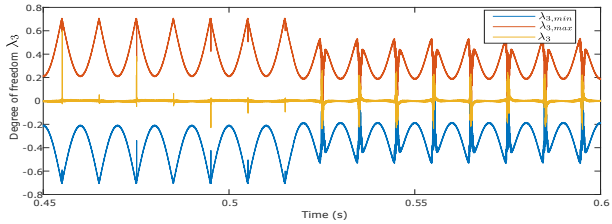

Fig. 7 Degree of freedom λ_3

As highlighted in Eq. (27), the reference voltage $V^*_{ao_{ref}}$ is an input to generate α. In the following, the reference voltage applied is:

$$V^*_{ao_{ref}} = V_{ao,max} \sin \omega_0 t + \frac{E}{2}, \tag{40}$$

where $V_{ao,max}$ is 70 % of $\frac{E}{2}$ and $\omega_0 = 2\pi f_0$.

To simulate the floating capacitance fault, a voltage unbalance is applied at $t = 0.5\ s$ across the capacitor C_1. To do so, a leakage current I_{leak} of 15% of the nominal load current is produced. I_{leak} flows through the resistance denoted R_1, placed in parallel to C_1. R_1 is sized such as $R_1 = \frac{V_{C1,ref}}{I_{leak}} = 100\ \Omega$. Consequently, a large imbalance of the v_{C1} voltage is caused by the injected disturbance. In usual PWM strategies, the voltage unbalance is not taken into account thanks to the PWM scheme. It is not the case with the proposed PWM strategy, where the d.o.f is dynamically adjusted, thanks to the v_{C_i} expressions.

The simulation results are given in figure 5, 6 and 7, which present the 3 d.o.f. before and after the default. It is illustrated that before the fault, the d.o.f are included within their boundaries and equal 0. The spikes are due to the current value injected into Eq. (38), when its value is close to 0. After the default, the d.o.f is varying dynamically (except

if the d.o.f reaches one of its boundary). In such a case, it is set at the boundary value, as illustrated.

Figure 8 depicts the 4 duty cycles and Figure 9 presents the load current I_L and the load voltage v_{ao}. It is illustrated that, in any case, the proposed strategy keeps the duty cycles within the boundaries $0 \leq \alpha \leq 1$. The voltage unbalance compensation allows to get a correct and expected multilevel functioning, for the current and voltages. More precisely, the dynamic PWM leads to maintain the reference values for the intermediate voltage levels, whereas the load current is still a sinus. Moreover, to prove the performance of the dynamic PWM strategy, a Fast Fourier Transform (FFT) analysis is performed in both usual and proposed PWM schemes. For both PWM, the I_L FFT analyses are presented in Fig. 10 and Fig. 11, respectively. On the one hand, with the use of the dynamic PWM, the I_L spectrum analysis shows a low harmonic distortion rate (THD), equal to 3.33%. On the other hand, the I_L THD of the current increase to 5.07% in the case of the usual PWM.

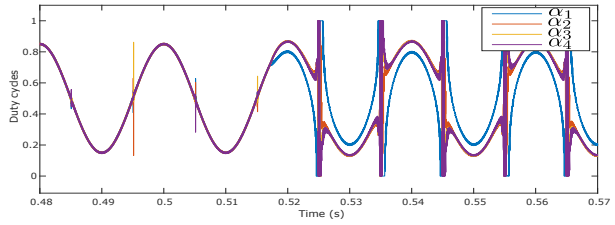

Fig. 8 Duty cycles α_i

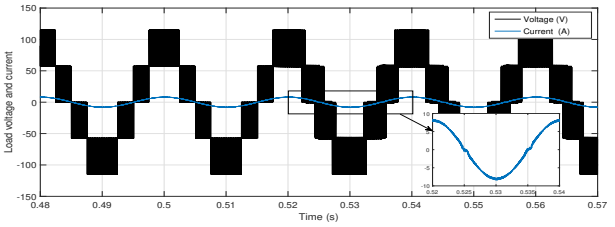

Fig. 9 Load voltage and current

6 Conclusion

A dynamic Pulse Width Modulation strategy is developed in this paper. A generic N-level Flying capacitor inverter mode is first introduced. Then, the dynamic PWM scheme is exhibited and applied to a 5-level single leg. It is demonstrated that the PWM scheme can embed the expressions of 3 degrees of freedom that are related to the floating capacitor voltages. More precisely, the capacitor voltage unbalance is dynamically set as a variable part of the duty cycle expressions. Simulation results demonstrate the performance of the proposed algorithm in the case of capacitor voltage unbalance. Also, this results have shown the performance and robustness of the proposed control strategy compared to the usual PWM.

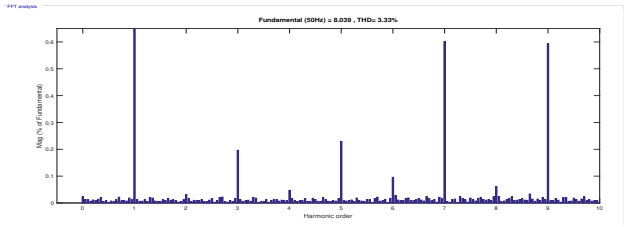

Fig. 10 FFT analysis of the load current for dynamic PWM

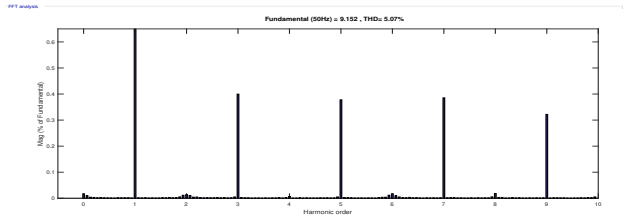

Fig. 11 FFT analysis of the load current for the conventional PWM

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