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Abstract

Over the last decade, the rating of photovoltaic power stations has increased progressively; however, they still operate at low voltage level. Hence, new architectures with an intermediate MVDC collector are investigated. This paper introduces a new topology of isolated DC/DC converter based on 1.7 kV and 3.3 kV SiC power modules, which allows the connection of PV arrays to the MVDC collector upstream from the MVAC distribution grid. As a prelude to the realization of a full-scale prototype, 1.7 kV SiC MOSFETs are characterized in both hard- and soft-switching condition. Finally, a study supported by simulations pointed out that the proposed converter shows a high efficiency (> 98.5%).

1 Introduction

Nowadays, due to the fast depletion of fossil fuels, most countries are considering the massive use of renewable energies [1]. Among them, photovoltaïc (PV) capacities increased considerably over the last decade [2][3]. As a result, PV stations of several hundred of megawatts are commonly built [4]. However, these stations are designed in low voltage levels, i.e. $1500V_{DC}$ for DC side (PV strings) and $800V_{AC}$ for AC side (LV/MV transformers). Given the involved power level and the level of efficiency to be achieved, these stations show numerous drawbacks, i.e. a high amount of power semiconductors, a significant use of copper and aluminum (cabling), more bulky 50/60-Hz transformers [5][6]. Consequently, a shift towards medium voltage (MV) levels on both DC and AC side is considered [7][8]. A MV topology for PV power stations is presented in Fig. 1. The inputs of isolated DC/DC converters are connected in parallel to a PV array while the outputs are connected in series, establishing an intermediate MVDC collector. A multilevel voltage source inverter (VSI) based on IGBTs is then directly connected to MVAC grid without any 50/60 Hz transformers.

Thanks to the availability of SiC power modules in MV ratings [9][10], medium frequency (MF) power electronic transformers (PETs) are now feasible, offering high efficiency as well as high power density [11]. From this perspective, the paper presents firstly a resonant topology selected to achieve the isolated DC/DC converter. Secondly, the switching characterization of the SiC MOSFET modules is carried out and electrothermal simulations are then performed with PLECS software in order to calculate the efficiency of the converter. Finally, the design of a 260 kVA prototype including a ferrite based dry transformer is presented.

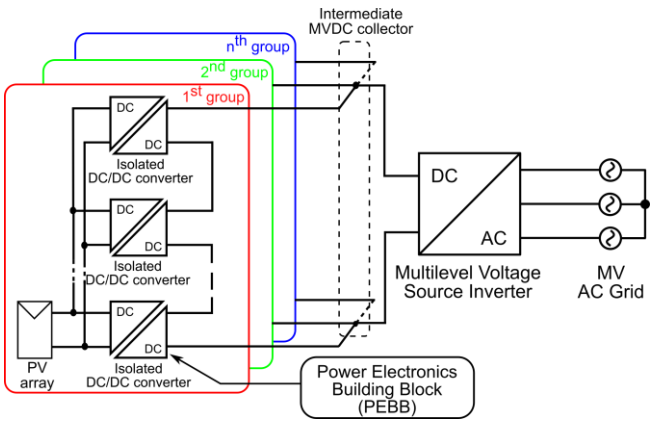


Fig. 1: A MV topology for large-scale PV plant [12]

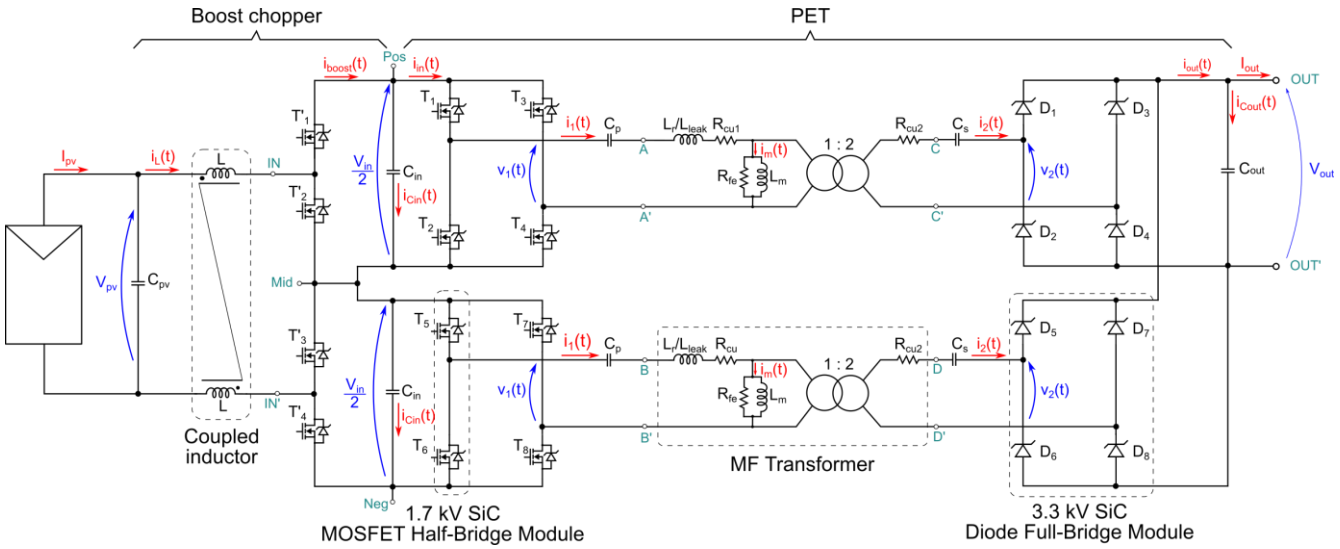


Fig. 2: 1.7 kV / 3.3 kV SiC Based PEBB in ISOP configuration

2 Power Electronics Building Block

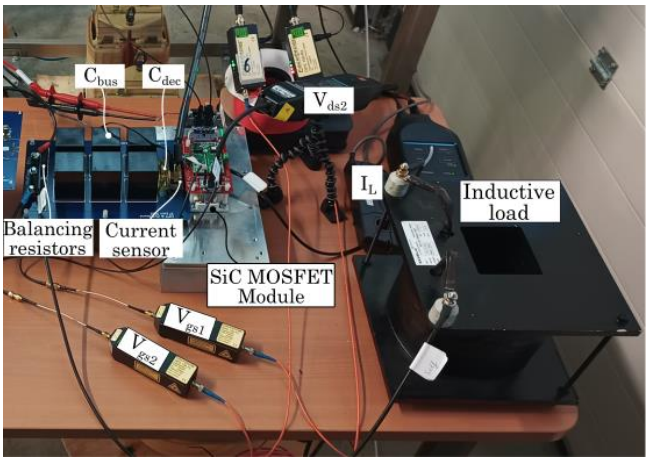
Fig. 2 presents the topology selected to build the isolated DC/DC converter. As shown in Fig. 2, the Power Electronics Building Block (PEBB) is composed of two cascaded conversion stages. Firstly, the Maximum Power Point Tracking (MPPT) is achieved by a boost chopper. Then, the galvanic isolation between the PV array and the MVDC collection feeder is achieved by a PET operating as a passive device like a transformer in AC power system. Since power flow is unidirectional in PV power generation, the most suitable topology is the Resonant Single Active Bridge (R-SAB) converter operating in Discontinuous Conduction Mode (DCM) [11][13][14]. In this mode, with a switching frequency lower than the resonant one, the MOSFETs of the inverter legs naturally operate in Zero-Voltage Switching (ZVS). In addition, the MOSFETs are turned off at the magnetizing current of the MF transformer which is relatively low, ensuring low switching losses.

The current voltage rating of commercial SiC devices allow the development of PV strings to an open-circuit voltage (V_{oc}) of 2 kV. As a result, the input and output voltage (i.e. V_{in} and V_{out}) of the PET was fixed at 2 kV. Thanks to the high availability of 1.7 kV MOSFET modules with improved packaging, the paper focuses on the topology using 1.7 kV/ 281 A SiC MOSFET Half-Bridge (HB) with very low stray inductance (3 nH) and 3.3 kV/ 90 A SiC diode Full-Bridge (FB) modules from Microsemi [15]. In order to adapt the voltage level, a three-level boost chopper is implemented. Its advantage is that the interleaved control of two switching cells (T_1', T_2') and (T_3', T_4') increases the frequency of the input current $i_L(t)$. Furthermore, the magnetic coupling of the two inductors limits their volume, and increases the power density of the PEBB. The isolated DC/DC conversion is then based on the input-series-output-parallel (ISOP) configuration of two R-SAB converters using MF transformers with a turn ratio of 2. This arrangement allows a natural voltage balancing at the input midpoint and no control loop is required [14].

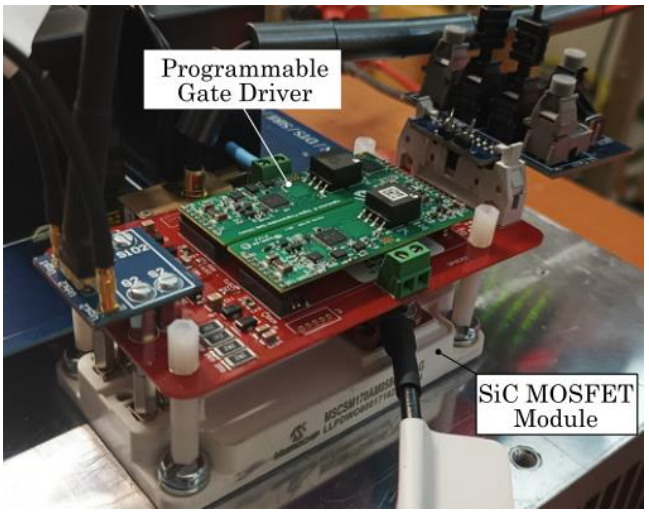
3 Switching characterization

The characterization of the SiC MOSFET power modules is necessary in order to have accurate thermal models for estimating the efficiency of the PEBB. The MOSFETs of the boost chopper operate in hard-switching condition while those of the R-SAB converters operate in ZVS condition. As a result, two different tests have to be carried out. Fig. 3 shows the switching characterization test bench. A power supply is connected to the MOSFET module via a PCB busbar and a set of capacitors. The bulk capacitors (C_{bus1},C_{bus2}) are sized to have the same value as those in the prototype (see section 5). High value resistors (R_1,R_2) are connected in parallel with the capacitors in order to have a good voltage balancing for the capacitive bridge. Then, decoupling capacitors (C_{dec1},C_{dec2}) are also implemented to minimise the stray inductance of the busbar. Concerning the gate control, internal and external gate resistance i.e. R_{Gint} and R_{Gext} are of 0.5 Ω and 1.1 Ω, respectively. An IZM ac-

tive shunt with the bandwidth (BW) from 70 kHz to 400 MHz and a sensitivity of 1.16 mV/A is used to measure the drain current I_{d2} [16]. For the voltage measurement, isolated probes are preferred. Hence, optical fibre probes are used, i.e. an IsoVu probe (BW = 800 MHz) [17] for V_{ds2} measurement and OPS probes (BW = 100 MHz) [18] for V_{gs1} and V_{gs2} measurements. Since the switching losses of SiC MOSFETs are independent of their junction temperature [19], the tests are realized under a same temperature of $25^{\circ}C$.



(a)



(b)

Fig. 3: (a) Switching characterization test bench; (b) Target module with gate driver [15]

3.1 Hard-switching characterization

The hard-switching characterization is achieved with classical Double-Pulse Tests (DPTs). Its electrical diagram is presented in Fig. 4. The Device Under Test (DUT) is the low-side (LS) switch. The MOSFET of the high-side (HS) switch is blocked. During the Turn-off of the DUT, the freewheeling sequence is achieved by the antiparallel SiC diode of the HS switch. The switching current of the DUT depends on the duration of the first pulse. Turn-off and turn-on energies (E_{off} and E_{on}) are then calculated at falling edge of the first pulse and the rising edge of the second one, respectively.

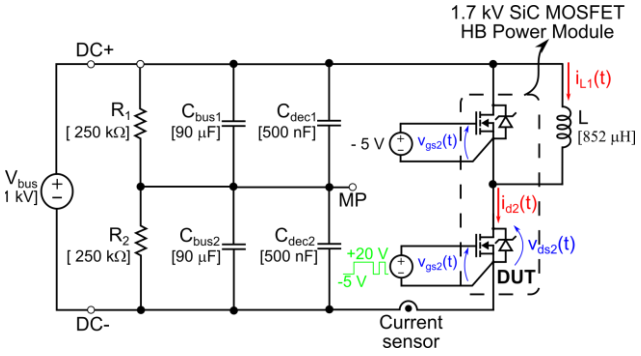
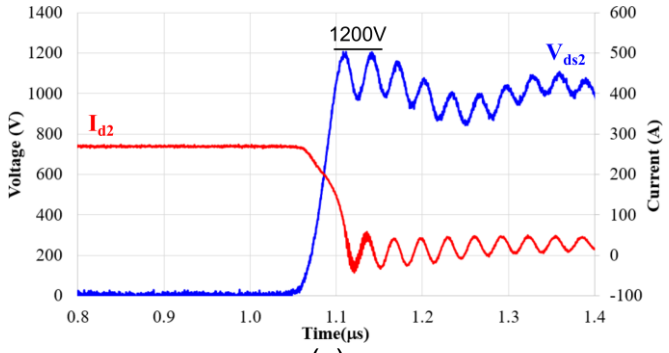


Fig. 4: Electrical diagram of the Double Pulse Test bench.

The switching waveforms and measured losses of the DUT are presented in Fig. 5 and Fig. 6, respectively.



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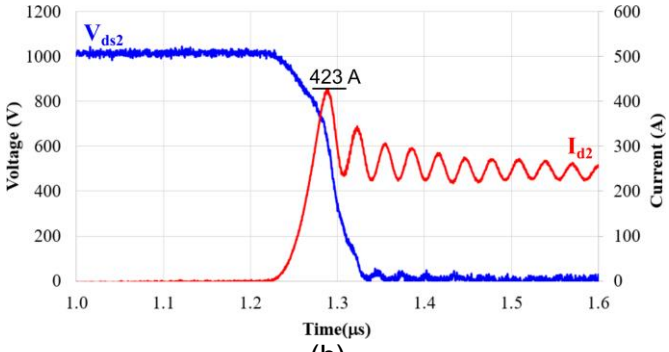
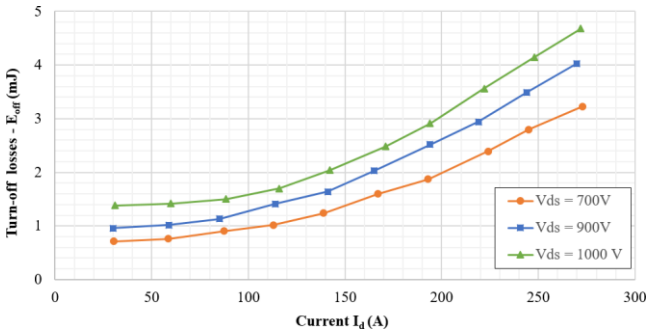
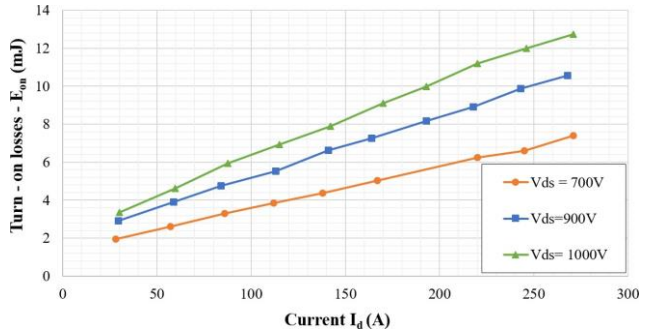


(b)

Fig. 5: Hard Switching waveforms at V_{bus} = 1000 V, I_{d2} = 270 A , R_{Gint} = 0.5 Ω, R_{Gext} =1.1 Ω, T_j = $25^{\circ}C$: (a) Turn-off; (b) Turn-on.



(a)



(b)

Fig. 6: Hard-switching mode - Switching energies as a function of the voltage and current: (a) Turn-off energies; (b) Turn-on energies.

3.2 Soft-switching characterization

The electrical diagram of the ZVS test bench is presented in Fig. 7. In this test bench, the ZVS operation is obtained by imposing a large dead time (t_{dead}) between the two control gate signals so that the forced Turn-on of the MOSFET takes place after the spontaneous turn-on of its antiparallel diode. The turn-off current is changed by modifying the switching frequency (f_{sw}) and can be calculated by Eq. (1).

$$I_{off} = \frac{V_{bus}}{8Lf_{sw}} \quad (1)$$

As stated in [20], during turn-on transition, a negative energy is measured. This corresponds to the energy exchanged between the parasitic capacitances C_{oss} of the switches. As a result, this energy cannot be considered as the losses. In hard switching condition with high current levels, this energy is not considerable in comparison with the switching losses. On the contrary, in soft-switching operation with low current level, this energy is not negligible. Hence, it should be substracted from the measured E_{off} in order to determine precisely the real losses

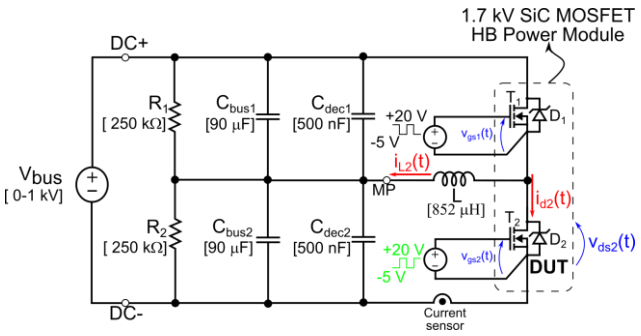
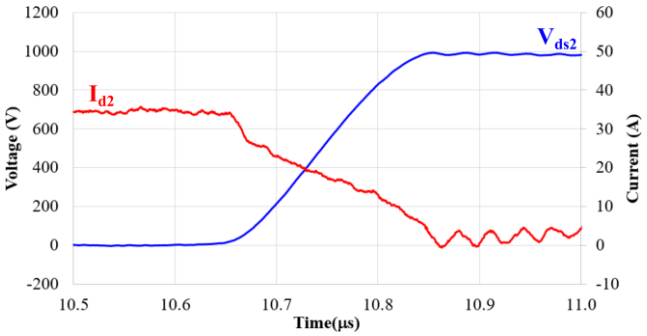


Fig. 7: Electrical schematic of ZVS test bench

as Eq. (2).

$$E_{off}(loss) = E_{off}(measured) - E_{off}(cap) \quad (2)$$

where: E_{off} (cap) - the exchanged energy during the controlled turn-off of the DUT.
The switching waveforms and energies of the DUT operating in ZVS condition are presented in Fig. 8 and Fig. 9, respectively.



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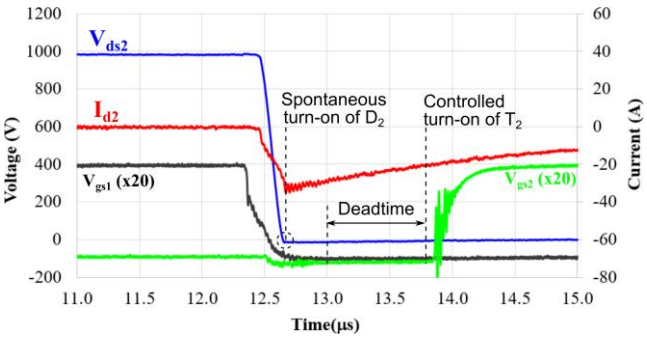

(b)

Fig. 8: Switching waveforms in ZVS mode at V_{bus} = 1000 V, I_{d2} = -33.7 A, t_{dead} = 1.5 µs: (a) Controlled turn-off of the MOSFET; (b) spontaneous turn-on of the diode.

4 Efficiency estimation

The efficiency estimation of the isolated DC/DC converter is carried out by simulations in PLECS

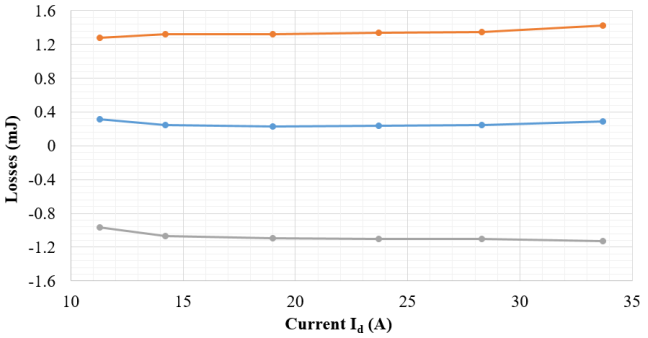

Fig. 9: LS switch turn-off energies as a function of the drain current I_d under ZVS operation (V_{ds} = 1000 V).

software [21]. In the thermal model of the power modules, the Switching Energy curves are set up from the measurements presented in the section 3. The static characteristics are those specified in the manufacturer datasheet. The winding and core losses of the MF transformers and coupled inductor (made by CEFEM Boige & Vignal, France [22]) are also taken into account considering constant electrical parameters as shown in Fig. 2. The specifications of the MF transformers and the coupled inductor are presented in Tab. 1 and Tab. 2, respectively.

Tab. 1: Specifications of MF transformers

Nominal apparent power (S_n)	130 kVA
Turn ratio	1:2
Operation frequency	20 – 30 kHz
Nominal primary voltage	1000 V
Nominal secondary voltage	2000 V
Primary resistance (R_{Cu1})	3 $m\Omega$
Secondary resistance (R_{Cu2})	16 $m\Omega$
Core resistance (R_{fe})	5.5 $k\Omega$
Leakage inductance (L_{leak})	15 μH
Magnetizing inductance (L_m)	1 mH
Magnetic material	Ferrite
Weight	30 kg

The simulations consider that the case temperature of the power modules is of $85^{\circ}C$. The input power is increased until the semiconductors reach their thermal limit or the transformers reach their nominal power. This operating point determines the nominal power of the PEBB. The voltage V_{pv} is varied at 1000 V to 1800 V corresponding to the MPP range of 2 kV PV strings operating between $85^{\circ}C$ and $-20^{\circ}C$. The simulation parameters are shown

Tab. 2: Specifications of coupled inductor

Leakage inductance (L)	350 μH
Nominal DC current	180 A
Winding resistance	3.7 $m\Omega$
Core resistance (20 kHz)	1.5 $m\Omega$
Magnetic material	Amorphous
Weight	40 kg

in Tab. 3. The efficiency of the boost chopper, the R-SAB converters and the complete isolated DC/DC converter as a function of the input power are presented in Fig. 10.

Tab. 3: Simulation parameters in PLECS software

Input DC bus voltage (V_{in})	2000 V
Output DC bus voltage (V_{out})	2000 V
PV voltage (V_{pv})	1000-1800 V
Switching frequency of T_i (i = 1..8)	20 kHz
Switching frequency of T_j' (j = 1..4)	10 kHz
Primary resonant capacitance (C_p)	3.8 μF *
Secondary resonant capacitance (C_s)	1.9 μF*
Case temperature of modules	85 $^{\circ}C$

*The choice of these values is detailed in Section 5.

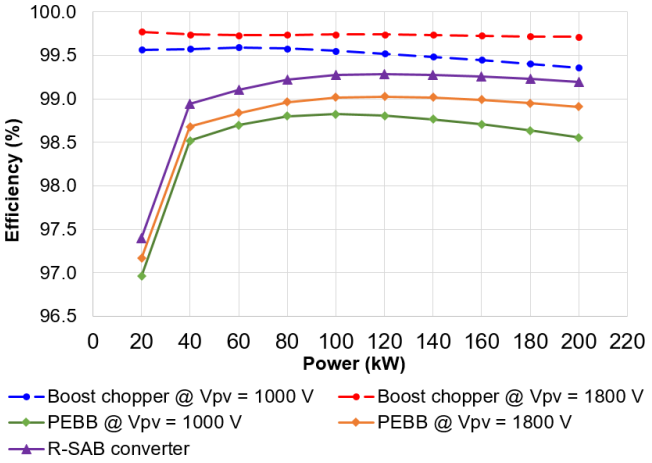

Fig. 10: Simulation results – efficiency of the PEBB, boost chopper, R-SAB converters .

Fig. 10 shows that both the two conversion stages offer high efficiency i.e. 99.5% for the boost chopper and 99.3% for the ISOP PET. Thanks to the DCM and ZVS operation, the power losses of the semiconductors are relatively low. As a result, the switches operate below their thermal limits. The nominal power of the PEBB is limited by that of

the MF transformers. Overall, the PEBB has an efficiency greater than 98.5% over 90% of the operating range. The maximum efficiency reaches 99% in case that the PV arrays are in favorable ambient condition i.e. high solar irradiance and low temperature.

5 Design of a prototype

In order to validate the simulation results, a full-scale prototype has been built. The following subsections describe the sizing of the devices of the PEBB.

5.1 Sizing of resonant capacitors

Resonant capacitors are installed on both side of the transformers in order to balance the overvoltages applied on the winding of the transformers (due to resonant effects). On the other hands, the leakage inductance L_{leak} of the MF transformers is used as the resonant inductance in order to optimize the PEBB layout. The calculation of C_p and C_s are based on their equivalent capacitance C_{eq} (referred to primary side of the transformers). Considering f_o – the resonant frequency, the value of resonant capacitors are calculated by Eq. (3).

$$f_o = \frac{1}{2\pi\sqrt{L_{leak}C_{eq}}} \quad (3)$$

In this prototype, the switching frequency f_{sw} of T_i ($i = \overline{1..8}$) is chosen to be 20 kHz. Then, the frequency ratio (f_{sw}/f_o) is chosen to be 0.8. As the windings of the transformer should have a same overvoltage, the value of C_p and C_s is of 3.8 μF and 1.9 μF, respectively. Other criteria of sizing the resonant capacitors is the RMS value of their voltage and current. By using PLECS software, the RMS value of the voltage and current of the resonant capacitors at the nominal power are presented in Tab. 4.

Tab. 4: Electrical quantities of resonant capacitors.

	Primary capacitor (C_p)	Secondary capacitor (C_s)
V_{rms}	226 V	226 V
I_{rms}	112 A	56 A

Considering the price and the delivering time, the authors worked with the capacitor manufacturer (CEFEM Power, France [23]) in order get custom-made samples that meets the specifications.

5.2 Choice of DC capacitors

The interleaving control between the R-SAB converters minimizes the voltage ripples on the output capacitor (C_{out}). Its sizing is based on the RMS value of its current $i_{Cout}(t)$ (see Eq. (4)) at the nominal power (P_n) of the PEBB.

$$I_{Cout} = I_{in}\sqrt{\frac{\pi^2 f_o}{8 f_{sw}}\left(\frac{P_n}{V_{in}}\sqrt{\frac{\pi^2 f_o}{8 f_{sw}}} - 1\right)} \quad (4)$$

Where I_{in} - DC component of the current $i_{in}(t)$.
On the other hand, the voltage ripples on the input capacitors (C_{in}) are induced by the harmonic currents resulted both from the boost chopper and the R-SAB converters. Despite the analytical calculation is still possible, it is complicated and time-consuming. As the results, the sizing of the capacitors C_{in} is determined by simulations in PLECS software. The specifications of C_{in} and C_{out} are presented in Tab. 5. The capacitance values are calculated considering a maximum voltage ripple at 5% of the DC voltage at the nominal power.

Tab. 5: Specification of DC capacitors for P_n = 200 kW

	C_{in}	C_{out}
C_{min}	46 μF	7.5 μF
V_n	1000 V	2000 V
I_{rms}	113 A	66.5 A

From a technological point of view, the DC capacitors have low capacitance but have to support high voltage and RMS current. Moreover, considering the fast switching characteristics of the SiC devices, these capacitors should have a stray inductance as low as possible to minimize the turn-off overvoltage. For the prototype, capacitors of the FFVE series from AVX manufacturer were selected [24]. Each capacitor C_{in} is composed of two devices connected in parallel to support the RMS current of 113 A while the capacitor C_{out} comprises only one device.

5.3 Prototype setup

In order to limit the thermal constraints on the semiconductors during the tests, the power modules are cooled by water plates. The PEBB is composed of

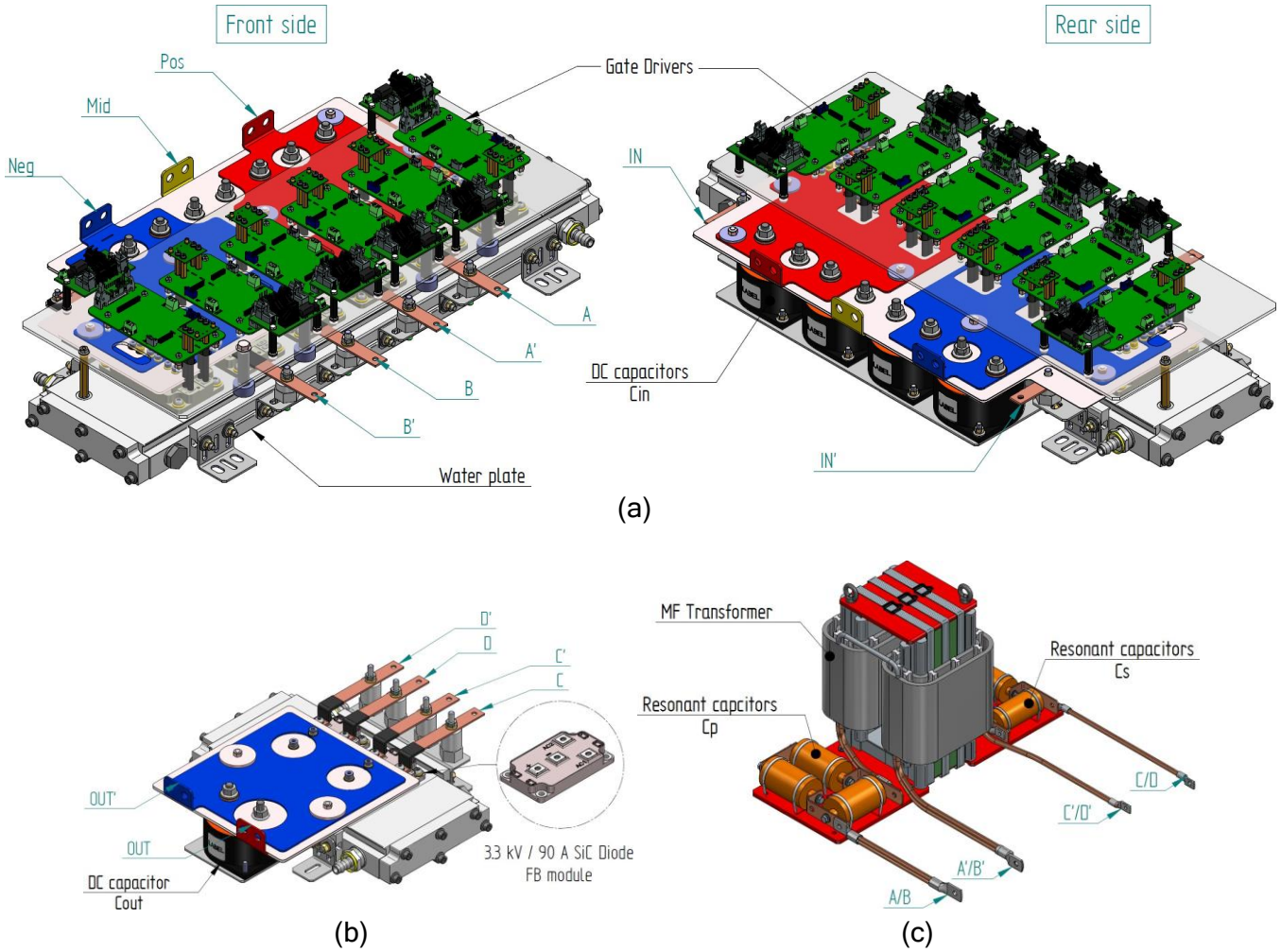

Fig. 11: Mechanical design of the PEBB: (a) Primary power stack; (b)Secondary power stack; (c) AC links.

two power stacks (designed and manufactured by ARCEL, France [25]) in which connections of power modules and DC capacitors is done by two stacked dual-layer laminated busbar. The latter helps minimizing the stray inductance in the switching loop. In the primary power stack, two MOSFET modules in the two side ends are used to realize the boost chopper while the others in the middle are used to for the R-SAB converters. Furthermore, the connection between the power stacks, the resonant capacitors and the MF transformers use Litz wires in order to minimize additional losses due to skin and proximity effects. The main parts of the PEBB are shown in Fig. 11.

6 Conclusion

In this paper, a new topology of isolated DC/DC converter comprising a three-level boost chooper and an ISOP PET was presented. The characterization of the 1.7 kV SiC MOSFET modules was carried out both in hard and soft switching conditions. Due to the presence of the non-negligible exchanging energy between the C_{oss} of the switches, the loss calculation in ZVS characterization should be carefully done in order to have accurate results. Then, the simulations with PLECS software pointed out that the proposed converter offers a high efficiency (> 98.5%) for over 90 % of operating range. Combining with the dry MF transformers with reduced mass and volume (see Tab. 1), the proposed PEBB has a high power density; and hence a strong potential to replace the bulky 50/60-Hz transformers in LV PV systems. This fact will make large-scale PV power plants more effective in terms of efficiency and cost. Finally, with the objective of validating the simulation results, a full-scale prototype is built and the choice of its main components has been detailed. The next step of this work will be assembling and testing this prototype.

7 Acknowledgement

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