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► **To cite this version:**

A.F. Hanna Nohra, Maurice Fadel, Hadi Y. Kanaan. A Comparative Study between a Conventional Two-Level and a Flying Capacitor Four-level VSI for Use in Four-Wire Shunt APF Applications. International Conference on Renewable Energies and Power Quality (ICREPQ'2016), May 2016, Madrid, Spain. pp.16-22, 10.24084/repqj14.211 . hal-03544202

HAL Id: hal-03544202

<https://ut3-toulouseinp.hal.science/hal-03544202v1>

Submitted on 26 Jan 2022

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A Comparative Study between a Conventional Two-Level and a Flying Capacitor Four-level VSI for Use in Four-Wire Shunt APF Applications

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Abstract. Shunt Active Power Filters (SAPF) are proposed for Power Quality (PQ) improvement in perturbed power distribution networks. Conventionally, the 2-level Voltage Source Inverter (VSI) topology is used in three-phase four wire power distribution networks to mitigate current harmonics and to enhance Power Factor (PF). The Multilevel Inverter (MI) such as the Flying-Capacitor (FLC) topology is competitive with the conventionally inverters for the same targets on low voltage domain, in addition to its performance in medium voltage. In this work a comparative study of two SAPF topologies is proposed. We compare the performance for the two structures for the same modulation, same current and voltage regulation method, same control strategy using modified formulation of the $p-q$ strategy. Firstly, it is demonstrated that the neutral current can be reduced in the conventionally 2-level structure by using a Phase Shift PWM (PSPWM) modulation instead of Sinusoidal PWM (SPWM) modulation. Secondly, peaks of source currents are reduced in the transient state by action on the Pass Band of the DC voltage regulator. Thirdly, comparison between the sizes of the inductance of the filters is made, voltage stresses on the electronic components are compared and harmonic generated by the output voltages of VSI are compared. It is demonstrated the superiority of the FLC over the two-level topology.

Keywords

Active power filter, VSI, FLC, modified $p-q$ theory, harmonics.

Nomenclature and Formulas

<i>SAPF</i>	Shunt Active Power Filter
<i>APF</i>	Active Power Filter
<i>PQ</i>	Power Quality
<i>VSI</i>	Voltage Source Inverter
<i>PF</i>	Power Factor
<i>MI</i>	Multilevel Inverter
<i>FLC</i>	Flying Capacitor
<i>PSPWM</i>	Phase Shift Pulse Width Modulation
<i>SPWM</i>	Sinusoidal Pulse Width Modulation
v_{inv}	Output voltage of the inverter
V_{inv}	Average value of the filter's output voltage
G_{inv}	Gain of the inverter
f	Frequency of the voltage source
f_{sw}	Switching frequency

<i>PB</i>	Pass Band
f_{PB}	Pass band frequency
<i>THD</i>	Total Harmonic Distortion

$$THD_x = \frac{\sqrt{\sum_{h=2}^{\infty} X_h^2}}{X_1}$$

1. Introduction

Nonlinear loads such, as televisions, compact fluorescent lamps, personal computers and multimedia devices, phone chargers and battery charger for electric vehicle in addition to more other tertiary sector and industrial loads, are increasingly used in power distribution networks. All this devices absorb a non-sinusoidal current that increases the current and voltage Total Harmonic Distortion (THD) [1-4], generates a noticeable circulating current in the neutral line [5], and causes additional losses in the power transmission lines and transformers [6-9]. It is demonstrated in [10] that the voltage distortion can exceed levels set by IEEE 519 [11] due to the progressive use of nonlinear devices.

The SAPF was already presented as a solution for improving PQ [12-21]. But researches are needed to improve the quality of filtering.

Pulse Width Modulation PWM [22-23], is used for a VSI and MI. In this paper, we propose the Phase Shift PWM (PSPWM) modulation scheme for the VSI based-on three carriers shifted of 120° like as the modulation control for a FLC. This control insures a good control for the neutral current on the side of the source and permits a fair comparison with the FLC.

And more, in this work, a comparison on the performance of the two structure is studied on term of sizing of filter inductance, on the harmonic distortion of source currents and finally on the electronic component constraints.

This paper is organized as follows. In section 2, the SPWM and PSPWM are presented but slightly modified in order to obtain the gain of converters. Consequently, the current regulation scheme is done. In section 3, DC voltage regulation and control law for both structures are presented.

In fact, a new control strategy was developed and validated in a previous work [24-25]. In this paper, just a summary is given about this control strategy.

In section 4 a comparison is made on the performance of SAPF on PSPWM modulation scheme and classical SPWM. It is demonstrated in this section that the PSPWM is better than the SPWM for active filter operation. More, performance of the simulation based on the Pass Band of the DC voltage regulator is discussed. Also, in this section, the comparison between conventionally VSI and FLC VSI is made. The simulation results using the Psim tool are presented and discussed. The paper finally ends with some concluding remarks in section 5.

2. Modulation Techniques

A. Sinusoidal PWM

In the classical SPWM, The VSI converter is controlled using one carrier modulation strategy compared to the three reference signals illustrated in Fig. 1.

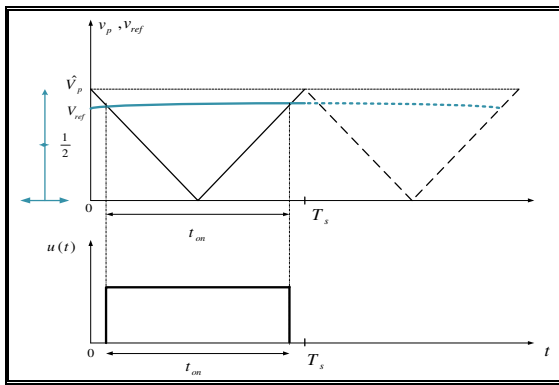


Fig. 1. PWM for one reference.

The average value of the control signal $u(t)$ on a switching period T_s is therefore:

$$\langle u(t) \rangle = \frac{1}{T_s} \int_0^{T_s} u(t) \cdot dt = \frac{t_{on}}{T_s} \quad (1)$$

The duty cycle is given by:

$$\alpha = \frac{t_{on}}{T_s} = \frac{V_{ref}}{\hat{V}_p} = \langle u(t) \rangle \quad (2)$$

The average value of the output voltage of the inverter v_{inv} on a switching period T_s is therefore:

$$V_{inv} = \frac{E}{2} (2 \cdot \alpha - 1) \quad (3)$$

Replacing (2) on (3) and assuming that:

$$\hat{V}_p = 1 \quad (4)$$

The average voltage of the inverter becomes:

$$V_{inv} = \frac{E}{2} (2 \cdot V_{ref} - 1) \quad (5)$$

We can make a translation of $\frac{1}{2}$ for the v_{ref} presented on Fig. 2.

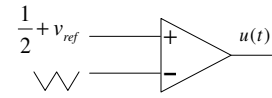


Fig. 2. Modification of v_{ref} .

The new reference is presented on Fig.3.

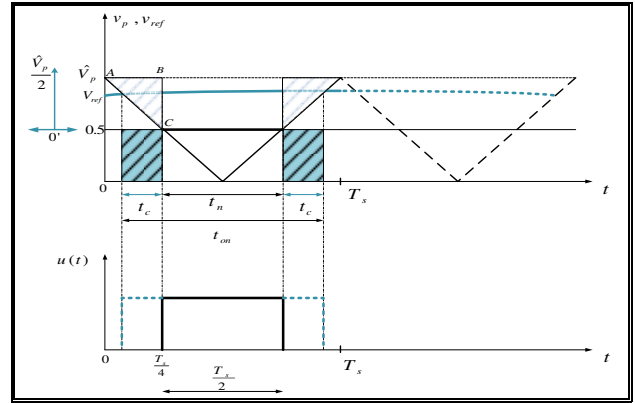


Fig. 3. Translation of the reference.

According to which we may set:

$$\alpha = \alpha_n + \alpha_{ref} \quad (6)$$

With, the naturally duty cycle:

$$\alpha_n = \frac{t_n}{T_s} = \frac{\frac{T_s}{2}}{T_s} = \frac{1}{2} \quad (7)$$

and:

$$\alpha_{ref} = \frac{2 \cdot t_c}{T_s} = \frac{V_{ref}}{\hat{V}_p} \quad (8)$$

Then:

$$\alpha_{ref} = \alpha - \frac{1}{2} \quad (9)$$

From (3) and (9), we can write:

$$V_{inv} = \frac{E}{2} (2 \cdot \alpha - 1) = \frac{E}{2} \left(2 \cdot \left(\alpha_{ref} + \frac{1}{2} \right) - 1 \right) = \alpha_{ref} \cdot E \quad (10)$$

Finally, by using (8) and (4) on (10), we obtain:

$$V_{inv} = V_{ref} \cdot E \quad (11)$$

The gain G_{inv} of the filter is:

$$G_{inv} = \frac{V_{inv}}{V_{ref}} = E \quad (12)$$

B. Phase shift PWM

For the VSI Fig. 9, the new command consists on employing three carriers shifted by 120 degrees and compared to the three reference signals. The resulting control signals $u_1(t)$, $u_2(t)$ and $u_3(t)$ are generated for each carrier. It is assumed that the switching frequency is much higher than the reference frequency.

For an FLC inverter with a three-cell structure, three carriers shifted by 120 degrees are employed and compared to the same reference signal. Three resulting control signals $u_1(t)$, $u_2(t)$ and $u_3(t)$ are generated. By assuming the switching frequency much higher than the reference frequency, the conducting periods of the switches are practically equal on a switching cycle T_s , i.e.:

$$t_{1on} = t_{2on} = t_{3on} = t_{on} \quad (13)$$

It yields:

$$\alpha_1 = \alpha_2 = \alpha_3 = \alpha \quad (14)$$

This assumption is essential for the operation of the FLC to ensure a natural balancing of the split DC voltages [39].

C. Electrical model for the filter

The electrical equation for the filter is:

$$v_{inv} - v_s = L_f \frac{di_f}{dt} \quad (15)$$

with:

$$v_{inv} = G_{inv} \cdot v_{ref} \quad (16)$$

These equations are represented by the block diagram in Fig. 4.

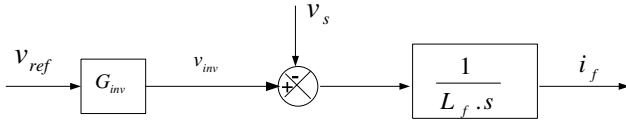


Fig. 4. Electrical model for one phase of the filter.

The grid voltage v_s constitutes a perturbation for the transfer function $\frac{i_f}{v_{ref}}$ which is compensated for as shown in Fig. 5.

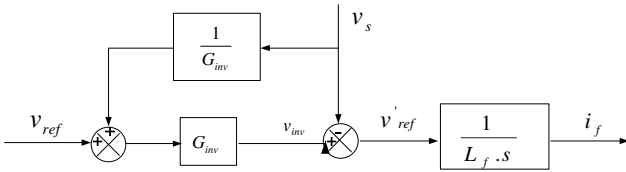


Fig. 5. Compensation of the source perturbation.

It yields:

$$v'_{ref} = \left(v_{ref} + \frac{v_s}{G_{inv}} \right) \cdot G_{inv} - v_s = v_{ref} \cdot G_{inv} \quad (17)$$

The transfer function can be then written:

$$\frac{i_f}{v'_{ref}} = \frac{1}{L_f \cdot s} \Rightarrow \frac{i_f}{v_{ref}} = \frac{G_{inv}}{L_f \cdot s} \quad (18)$$

Then:

$$\frac{i_f}{v_{ref}} = \frac{G_{inv}}{L_f \cdot s} = \frac{E}{L_f \cdot s} \quad (19)$$

3. DC Voltage Regulation and Control Strategy

A. DC voltage regulation

For the harmonics filtering and PF compensation, there is no need for energy storage on the capacitor. Otherwise, the capacitor would need an active power to replace energy used to compensate the losses on the filter. This leads to stabilize the DC bus voltage. The energy stored on the capacitor is:

$$w = \frac{1}{2} \cdot C \cdot V^2 \quad (20)$$

That gives for the instant power:

$$p = \frac{dw}{dt} = \frac{1}{2} C \cdot \frac{dV^2}{dt} \quad (21)$$

By setting:

$$X = V^2 \quad (22)$$

it yields:

$$p = \frac{1}{2} C \cdot \frac{dX}{dt} \quad (23)$$

and, in the Laplace domain:

$$P(s) = \frac{1}{2} C \cdot s \cdot X(s) \quad (24)$$

The transfer function is:

$$\frac{X(s)}{P(s)} = \frac{2}{C \cdot s} \quad (25)$$

On the other hand, the total power absorbed at the source for the two capacitors is:

$$P = \frac{3 \cdot \hat{V} \cdot \hat{I}_f}{2} = \frac{3 \cdot \hat{V} \cdot \hat{I}_f}{2} \quad (26)$$

For one capacitor:

$$P = \frac{3 \cdot \hat{V} \cdot \hat{I}_f}{4} \quad (27)$$

The block diagram in Fig. 6 illustrates this regulation, with:

$$k_p = \frac{2 \cdot C \cdot \omega_{PB}}{3 \cdot \hat{V}} \quad (28)$$

and:

$$T_i = \frac{\sqrt{10}}{\omega_{PB}} \quad (29)$$

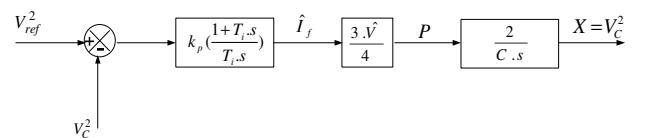


Fig. 6. Bloc diagram for the regulation of the DC voltage.

B. Control strategy

A new expression of the reference currents is developed in the method described in [24-25]. This method is based on

the separation of the zero sequence current from the zero sequence power in the case of balanced voltages and unbalance and distorted currents, which has permitted to control an equal repartition of the zero-sequence current component within the three phases of the supply distribution network yielding, thereby, the elimination of the neutral current. A brief description of this method follows.

Powers in the $\alpha\beta$ frame are given by the following equation:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (30)$$

Current references in $\alpha\beta$ frame are consequently given by:

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \cdot \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} \tilde{p} + p_c \\ -(\tilde{q} + \tilde{q}) \end{bmatrix} \quad (31)$$

The current references in abc frame are computed as:

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 0 & 1 & 0 \\ 0 & -1 & \frac{\sqrt{3}}{2} \\ 0 & -1 & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} + \begin{bmatrix} \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_n \\ 0 \\ 0 \end{bmatrix} \quad (32)$$

The block diagram in Fig.7 illustrates this method, where P_c represents the losses power. Fig. 8 represents the scheme of the regulation of current.

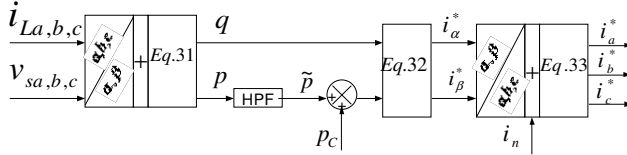


Fig. 7. Block diagram for reference currents extraction.

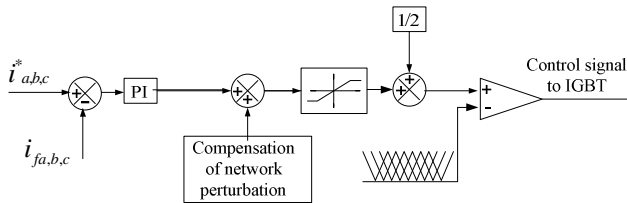


Fig. 8. Block diagram for current regulation and modulation.

4. Simulation Results and Discussions

All experiments are made with the following numerical values:

- Source: $\hat{V} = 310V, f = 50Hz$
- 2-level VSI inverter : $C = 1 mF, L_f = 12 mH$
- FLC inverter: $C = 1 mF, L_f = 2 mH$
- Modulation frequency: $f_{sw} = 10 kHz$
- Regulators: $f_{pb} = 3kHz, f_{pbv} = 300 Hz$
- Resistive loads: $R_{1a} = 6\Omega, R_{1b} = 8\Omega, R_{1c} = 10\Omega$
- Common load: $L_1 = 6 mH, R_2 = 0.5\Omega, L_2 = 20 mH, C = 1500\mu F$

A. Effect of the voltage loop crossing frequency

A good filtering is the result of a compromise between the method of reference currents extraction, modulation and regulators for currents and voltages. In what follows, we consider that the current absorbed by the capacitors, for the compensation of losses, is passed through the diodes of the inverter and its frequency is $6f$. Then, the crossing frequency of the DC voltage regulator is chosen for $f_{pbv} = 300Hz$. Fig. 9 illustrates the three levels FLC based on APF.

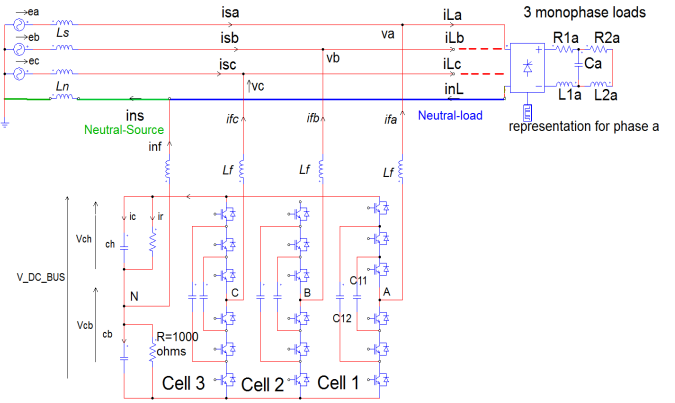


Fig. 9. Three cells, four-wire, four-level FLC APF.

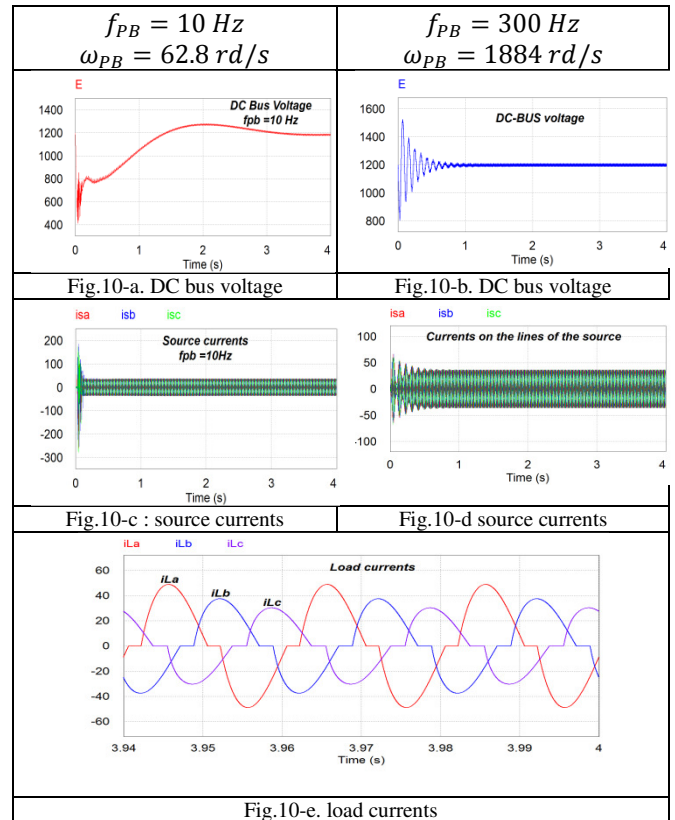


Fig. 10. Impact of the pass band of DC voltage regulator.

In Fig. 10, a comparison between two crossing frequencies for the voltage regulator shows that $f_{pbv} = 300 Hz$ (Figs. 10.b and 10.d) is better than $f_{pbv} = 10 Hz$ (Figs. 10.a and 10.c). For a smaller crossing frequency, the time response for the DC-bus voltage is obviously longer, and

the peaks on source currents are greater. In the following, $f_{pbv}=300\text{ Hz}$ is adopted for simulations. In Fig. 10.e, the load currents are show and, in Table 2, their THD values are given.

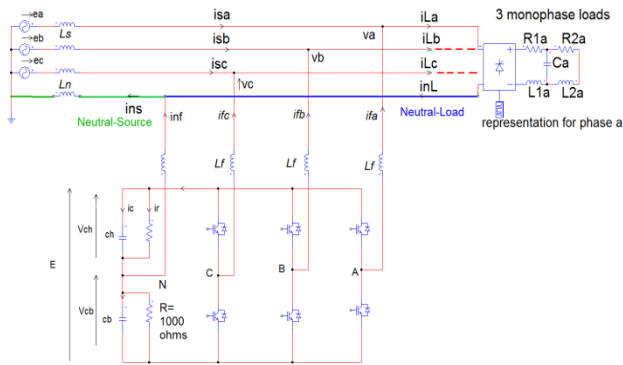


Fig. 11. VSI 2-level scheme on APF application.

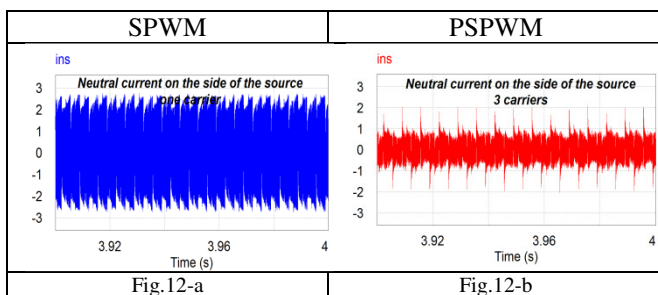


Fig. 12. Comparison between neutral currents.

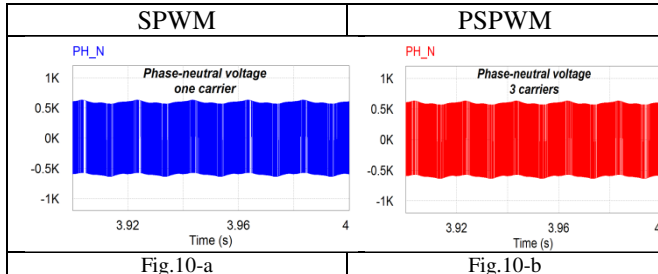


Fig. 13. Comparison between phase-neutral voltages for the two modulation techniques.

B. Comparison between the SPWM and PSPWM

The signal references for the APF come from the current regulator and they are perturbed. In the case where one carrier is used for the three references, we don't have precision on times commutation. It is for this reason that we use three carriers, one for each signal reference, that yielding for a better control for the neutral current.

Fig. 11 represents the VSI on APF application for four wire power distribution network.

In Fig. 12, neutral currents on the side of the source are compared for the tow modulation techniques. It is shown that the PSPWM offer a good control for the neutral current Fig.12.b.

In Fig. 13, the phase-to-neutral voltage are also compared and that show that no big modification on the output voltages. But in Table 1 and Table 2, values of harmonics components and respectively the THD values of source

currents give an advantage for the PSPWM. All these results highlight the superiority of the PSPWM over the SPWM for a VSI in APF application.

C. Comparison between the VSI and FLC

Once we have the same modulation, the same control strategy and the same voltage regulator, the comparison on the structures is fairly carried and gives a better appreciation. The main difference is on the size of the filter inductance. Fig.14 shows that the performance of the two structures cannot be approached except for a value of filter inductance for the 2-level equal to 6 times that of the FLC. Figs. 14.a and 14.b show the source currents for, respectively, 2-level and FLC and in Table 2, the THD values prove the excellent advantage of the FLC. In Fig. 14.d, neutral current on the source side for an APF based-on FLC is more reduced than that the neutral current for 2-levels VSI on Fig. 14.c. Harmonic contents within the phase to neutral voltage Figs. 14.e and 14.f are in the interest of the FLC and more, the first harmonic appears at $3f_{sw}$ for the FLC in Fig.14.f and at f_{sw} in Fig.14.e for the 2-level topology. In Fig.14.g and Fig. 14.h, the spectrum of the IGBT voltage shows that amplitudes of harmonics in the FLC (200 V for DC component) are lower than that the 2-level (600V for DC component). This result means that the harmonic stress on the IGBT of FLC topology is much reduced. It is a main advantage for a multilevel inverter.

5. Conclusions

In this work, a comparison is made between two topologies of VSI for SAPF application. It is validate by simulation for the FLC use that the neutral current on the side of the source is reduced more than that the 2-levels. Harmonic distortion of the source currents is also more reduced. These results are obtained with initially improvement for the functioning of the 2-level by using the PSPWM instead the SPWM modulation. The size of the filter inductor for a FLC is much smaller than that the 2-levels. Small amplitude of harmonic on the output voltage of the filter and the frequency of the first harmonic ($3xf_{sw}$) for the FLC leads to sizing a small output filter. The maximum of the voltage across IGBTs is reduced three times for the FLC versus the 2-levels. The FLC topology is shown to be better than the 2-level conventional inverter for APF applications.

Acknowledgements

This work has been supported by the National Council for Scientific Research, Lebanon (CNRS-L), the Agence Universitaire de la Francophonie (AUF), the PHC CEDRE 2014 project N°30108XK, the Research Council of Saint-Joseph University, Beirut, Lebanon, and the laboratory LAPLACE. The authors also wish to thank gratefully the Institut Français of the French Embassy in Lebanon and the Institut Supérieur des Sciences Appliquées et Economiques (I.S.S.A.E-Cnam Liban) for their financial contribution.

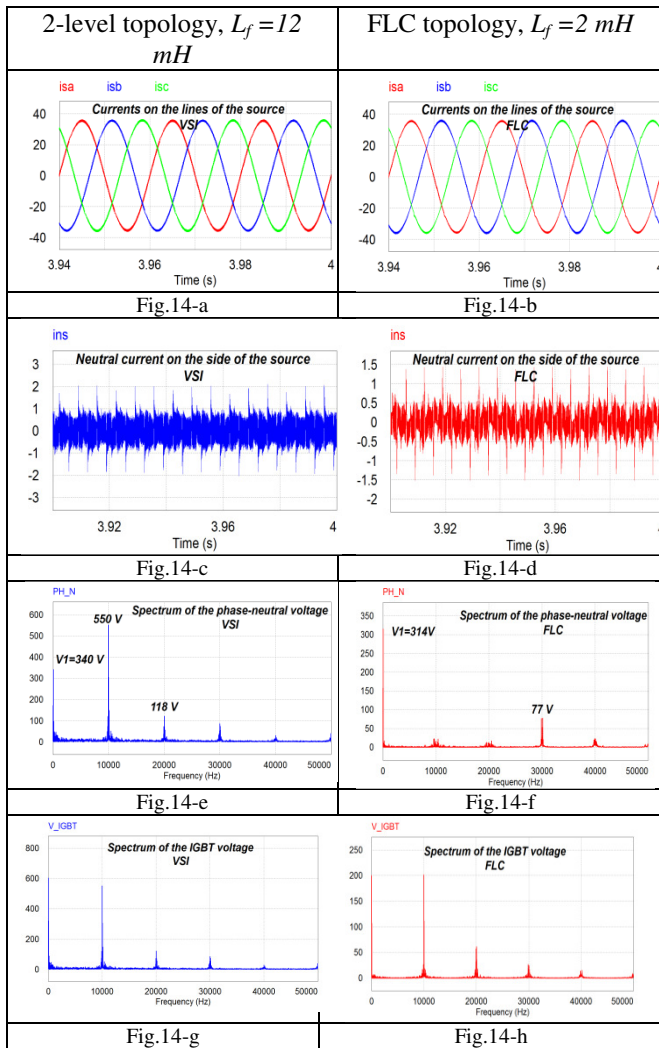


Fig. 14. Comparison between a VSI 2-levels and FLC.

Table 1: Harmonic components for the phase to neutral voltage.

Phase –neutral voltage		
harmonics	SPWM	PSPWM
50Hz	338	340
150 Hz	91	90
250 Hz	32	35
350 Hz	54	31
450 Hz	36	14
550 Hz	60	50
10 kHz	558	551
19950	74	73
20050	126	118

Table 2: Comparative values of THD for the source currents.

Load currents	THDi	Source currents	SPWM	PSPWM	PSPWM
			2-level	2-level	FLC
			THDi	THDi	THDi
iLa	17%	isa	2.35%	2.29%	1.42%
iLb	18%	isb	2.32%	2.24%	1.49%
iLc	19%	isc	2.36%	2.29%	1.38%

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