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# Direct modulation of electrical conversions for a multilevel chopper

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## Keywords

Multilevel converters, converter modelling, modulation strategies, converter control

## Abstract

In this paper the methodology of the Causal Oriented Graph (COG) is used for the modelling of a flying capacitor cell chopper. The issues of this study is a best understanding of the operating of this particular converter in order to obtain a more precise design of the control system. The obtained modelling shows that high-voltage multi levels are obtained by combination of two different three-level functions (conversion functions). Therefore a novel PWM strategy is deduced. It consists of separating the modulation period for creating two fictive modulated voltage systems via the direct width modulation and the position setting of both conversion functions. The redundancy of the different switches configurations for the voltage half value allows to use a particular modulation technique which limits the deviations of the half-value voltage. Switching patterns are deduced and a decoupling control of the capacitor voltage and the supply current is designed.

## 1. Introduction

Due to the incisive competition in mass transportation many innovations are considered and experimented for the economic improvement of the railway traction system. A main aspect is in the use of new and more powerful electrical drives. Recently, in the context of the reduction of the filtering elements, the replacement of the classical chopper (fig.1) by a flying-capacitor structure operating in voltage multilevel has been investigated [1]. It enables a diminution of the high-voltage harmonic magnitude and, in addition, the obtained blocking voltage of force-commuted semiconductor devices are least.

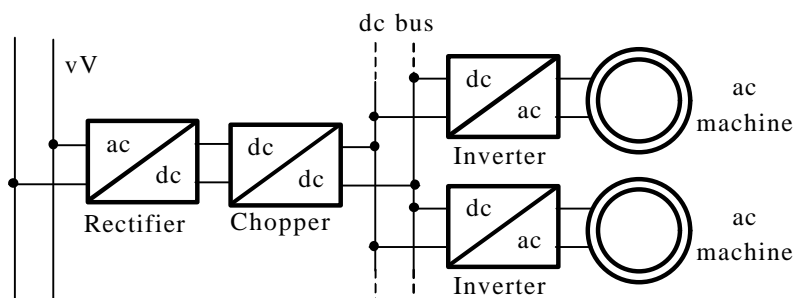


Fig. 1: Simplified representation of the power architecture

The power structure of the considered multilevel converter is composed by two elementary commutation cells with an intermediary capacitor (fig. 2). Each switching cell is made of one transistor and one diode in order to obtain an unidirectional power flow. To enable a PWM operating, the transistor and the diode of the same cell are assumed to be in complementary states.

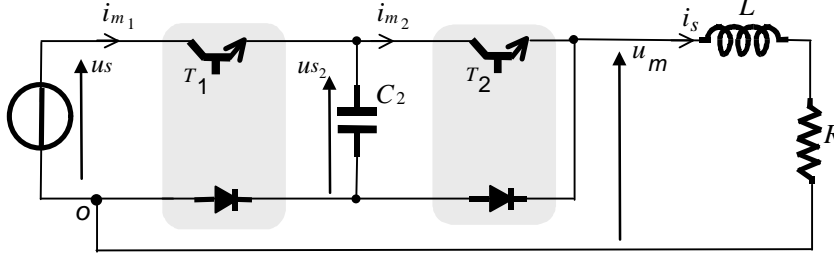


Fig.2 : Power structure of the flying capacitor converter

The converter is fed by a dc current-source controlled voltage rectifier and so the voltage source ( $u_s$ ) is constant. Two outputs will be considered: the supply current ( $i_s$ ) which is influenced by the modulated multilevel voltage ( $u_m$ ) and the capacitor voltage ( $u_{s2}$ ) which is influenced by two modulated currents ( $i_{m1}$ ,  $i_{m2}$ ). A high electrical coupling exists and make difficult in practice the instantaneous dc control of both outputs [2]. Our attention is being directed towards enhancing the performance of the control system.

So the section 2 is devoted to the analysis of the electrical conversions. The effect of switching connections is studied. A precise mathematical modelling is established for the analysis in real time of electrical conversions and the study of the multilevel operating. An averaged modelling is established for the study of filtered electrical quantities.

In section 3, the COG methodology is recalled and a graphical representation of all physical phenomena is obtained. Therefore the architecture of the control system is obtained by a graphical inversion of the causality path.

Two pulse width and position modulators are proposed and are described in section 4.

Then the design of the pulse width modulation and the position setting of three-level pulses in order to hold the capacitor balancing and the control of the supply current is explained in section 5.

In the last section simulation results on a ? V, ? kVA prototype are given.

## 2. POWER INVERTER MODELLING

### Effect of connections

The two commutation cells imply four different configurations of switches and modulated levels. So, they are coded by four connection functions which are called  $f_c$ ,  $c \in \{1,2,3,4\}$  (table 1).

Patterns	$T_1$	$T_2$	$f_1$	$f_2$	$f_3$	$f_4$	$u_m$	$i_{m1}$	$i_{m2}$
1	1	1	1	0	0	0	$u_s$	$i_s$	$i_s$
2	0	1	0	1	0	0	$u_{s2}$	0	$i_s$
3	1	0	0	0	1	0	$u_s - u_{s2}$	$i_s$	0
4	0	0	0	0	0	1	0	0	0

Table 1:

From this table we deduce the following expression of the modulated voltage :

$$u_m = f_1 \cdot u_s + f_2 \cdot u_{s2} + f_3 \cdot (u_s - u_{s2}) \quad (1)$$

And modulated currents are expressed as :

$$i_{m1} = (f_1 + f_3) \cdot i_s \quad (2)$$

$$im_2 = (f_1 + f_2) \cdot is \quad (3)$$

Connection functions are easily deduced from gate signals by following logic relations :

$$\boxed{f_1 = T_1 \cdot T_2, f_2 = \bar{T}_1 \cdot T_2, f_3 = T_1 \cdot \bar{T}_2, f_4 = \bar{T}_1 \cdot \bar{T}_2} \quad (4)$$

And, we can force values of wished connection functions ( $f_{c\_ref}$ ) by setting the corresponding gate signals of transistors following :

$$\boxed{T_1 = f_{1\_ref} + f_{3\_ref}, T_2 = f_{1\_ref} + f_{2\_ref}} \quad (4)^{-1}$$

### Conversion modelling :

The modulated voltage can be viewed as the result of the conversion of two voltage sources as :

$$um = um_1 + um_2 \quad (5)$$

with

$$um_1 = (f_1 + f_3) \cdot us, \quad (6)$$

and

$$um_2 = (f_2 - f_3) \cdot us_2 \quad (7)$$

If capacitor voltages have constant values, it appears that the voltage  $um$  is shaped through two conversion functions as :

$$um_1 = m_1 \cdot us \quad (8)$$

$$um_2 = m_2 \cdot us_2 \quad (9)$$

with

$$m_1 = f_1 + f_3, \quad (10)$$

$$m_2 = f_2 - f_3 \quad (11)$$

We have so defined two different functions whose position and width may be modulated. In a same way, we can express the two modulated currents as:

$$im_1 = m_1 \cdot is \quad (12)$$

$$im_2 = (m_1 + m_2) \cdot is \quad (12b)$$

### Analysis of multilevel operating :

All obtained voltage levels in unbalancing condition are listed into table 2. These ones are reduced to three voltage levels in balancing operation ( $us = us_2/2$ ).

Patterns	$T_1$	$T_2$	$f_1$	$f_2$	$f_3$	$f_4$	$um$	$m_1$	$m_2$	$im_1$	$im_2$
1	1	1	1	0	0	0	$us \rightarrow us$	1	0	$is$	$is$
2	0	1	0	1	0	0	$us_2 \rightarrow 1/2 \cdot us$	0	1	0	$is$
3	1	0	0	0	1	0	$us - us_2 \rightarrow 1/2 \cdot us$	1	-1	$is$	0
4	0	0	0	0	0	1	$0 \rightarrow 0$	0	0	0	0

Unbalancing condition
Balancing condition

Table 2:

$$m_1 \in \{0,1\}, m_2 \in \{-1,0,1\}$$

We can notice that equations (5), (8) and (9) control the application of the full level ( $us$ ) or the half level ( $us_2$ ).

### Modelling of the capacitor supply and the load

The dc voltage across the capacitor  $C_2$  results from two modulated currents (fig. 3) as:

$$i_{c_2} = im_1 - im_2 \quad (14)$$

and is given by :

$$u_{s_2} = \frac{1}{C_2} \int_{D_t} i_{c_2} dt + u_{s_{2\_0}} \quad (15)$$

where  $u_{s_{2\_0}}$  is the initial voltage load of the capacitor  $C_2$ .

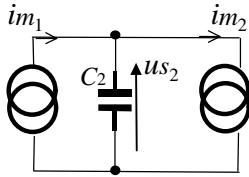


Fig. 3: Capacitor supply

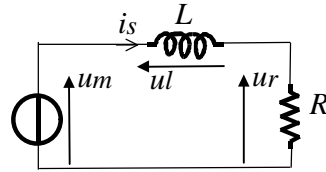


Fig. 4: Load supply

For the ease of explanation, the load is assumed to be a resistor and then we can consider that the multilevel voltage is applied to a first order filter (fig. 4). The classical electric equations are listed below.

$$ul = um - ur \quad (18)$$

$$ur = r \cdot is \quad (19)$$

$$is = \frac{1}{L} \int_{D_t} ul dt + is_{\_0} \quad (20)$$

where  $is_{\_0}$  is the initial current load of the inductor.

The set of these relations can be gathered and represented by a global relation (named (21)) whose the input is the modulated voltage ( $um$ ) and the output the current ( $is$ ).

$$is = \frac{1}{L} \int_{D_t} (um - ur) dt + is_{\_0} \quad (21)$$

### Averaged modelling

The purpose of the control system is to regulate the mean value of the modulated voltage ( $\langle um \rangle$ ) inside each modulation period in order to get a constant value of the load current ( $is$ ). The mean value of the modulated voltage during the modulation period ( $Te$ ) is expressed as:

$$\langle um(t) \rangle = \left[ \frac{1}{Te} \cdot \int_{k \cdot Te}^{(k+1) \cdot Te} um(t) dt \right]_{Te \rightarrow 0} \quad (22)$$

with  $k \in \mathbb{N}$ .

This quantity is linked to conversion functions and voltage sources (9) and (8) which are assumed to be nearly constant during the modulation period:

$$\langle um \rangle = \langle m_1 \rangle \cdot us + \langle m_2 \rangle \cdot us_2 \quad (23)$$

The mean value of a conversion function is therefore defined as :

$$\langle mr(t) \rangle = \left[ \frac{1}{Te} \cdot \int_{k \cdot Te}^{(k+1) \cdot Te} mr(t) dt \right]_{Te \rightarrow 0} \quad (24)$$

### **3. CONTROL ARCHITECTURE**

The ordering of all implicated relations following the input output transfer and the causality respect gives the representation depicted fig. 6.

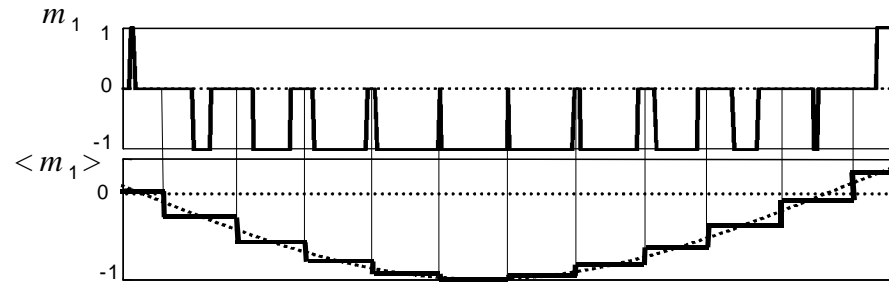


Fig. 5: Average modelling of conversion function

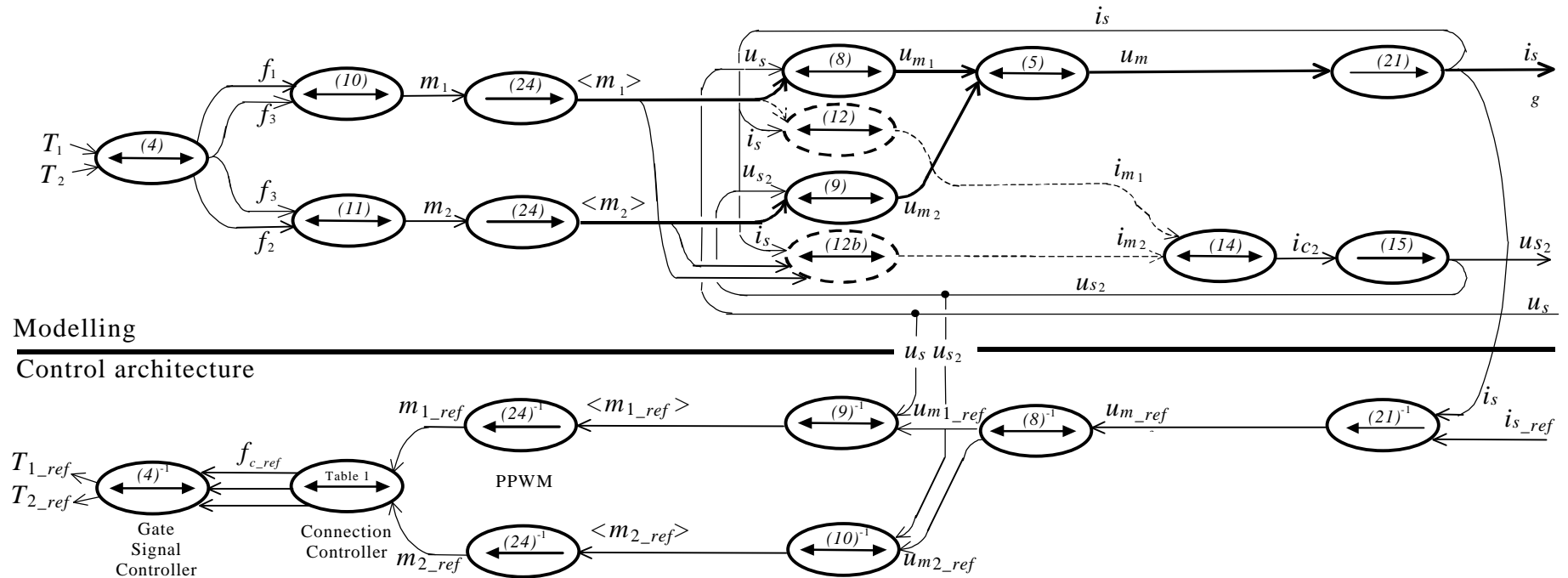


Fig. 6: COG of the flying capacitor chopper

Relations are represented by a balloon with inside it number. Causal relations are characterized by an integration operator and so contain an unidirectional arrow. Other ones contain a bi-directional arrow which means the existence of a direct inverse relation.

From this representation, we see that the current ( $i_s$ ) can be regulated to a reference ( $i_{sref}$ ) by a correct setting of the modulated voltage ( $u_m$ ) by a closed loop control whose relation is named  $(21)^{-1}$ . This multilevel voltage is built by two other modulated voltages ( $u_{m1}$  and  $u_{m2}$ ) which will be set through two conversion functions ( $m_r$ ). This freedom degree will be used to calculate conversion functions in order to hold a constant value of the capacitor voltage ( $u_{s2}$ ).

The average modelling produces equivalent continuous conversion functions ( $\langle m_r \rangle$ ) of discontinuous conversion functions. On the other hand, in the control system, we will have to produce a discontinuous reference conversion function ( $m_{r\_ref}$ ) from a desirable continuous reference conversion function ( $\langle m_{r\_ref} \rangle$ ). This is implemented by two pulse position and width modulators (PPWM) because this technique keep unchanged the mean value of discrete and continuous functions during a modulation period.

Finally, a logic connection controller processes the switching signals via an inverse mapping of table 2.

#### 4. PULSE WIDTH AND POSITION MODULATION

As shown fig. 7, two pulse width and position modulator (PPWM) are required to build conversion references from average conversion references (continuous signals) by mean of the conservation of the averaged value.

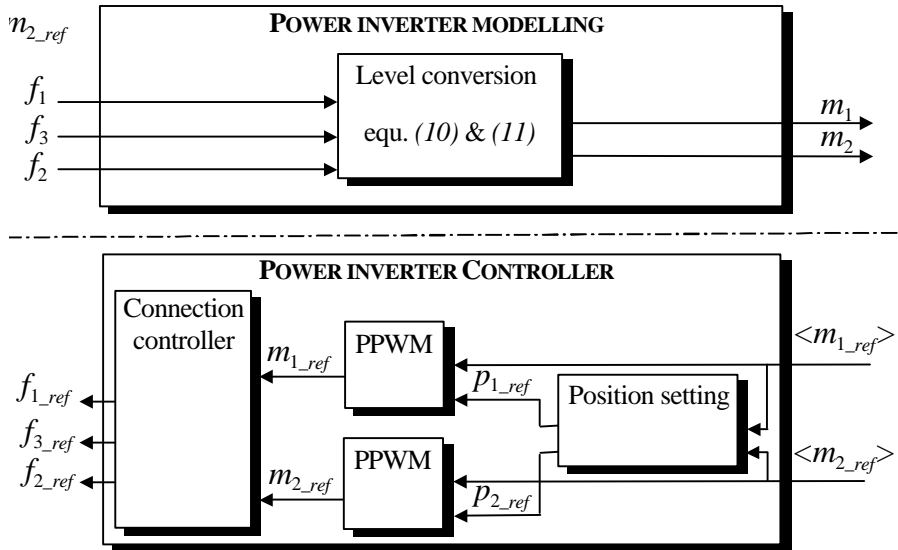


Fig. 7: Parallel PPWM

Previously, the operating of this modulator has been described by Petri nets [3]. Each modulator is able to locate the pulse in the modulation period. Each pulse position ( $p_1$  and  $p_2$ ) is calculated by a "Position setting" block which takes into account the available place and possible wrong patterns (as example  $m_{1\_ref} = m_{2\_ref} = 1$ ). With such modulators, reference conversion functions are made equal to mean value conversion functions :  $\langle m_{r\_ref} \rangle = \langle m_r \rangle$ .



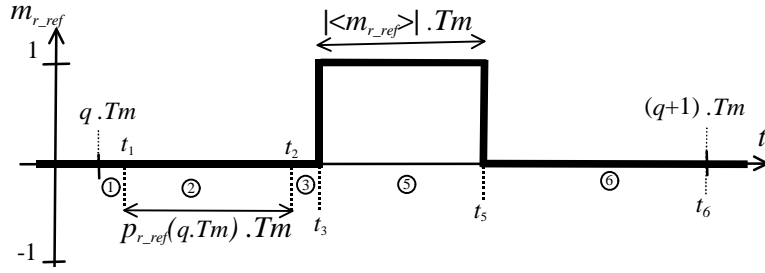


Fig. 8: Real time evolution of the modulated signal

## 5 ALGORITHM CONTROL

### Control of the load current

Our modulation system has been designed in order to make equal the mean value of the modulated voltage ( $\langle um \rangle$ ) to a reference ( $\langle um_{ref} \rangle$ ). The figure () represents the schema block of the system. The algorithm control of the current has been done with the help of three control actions.

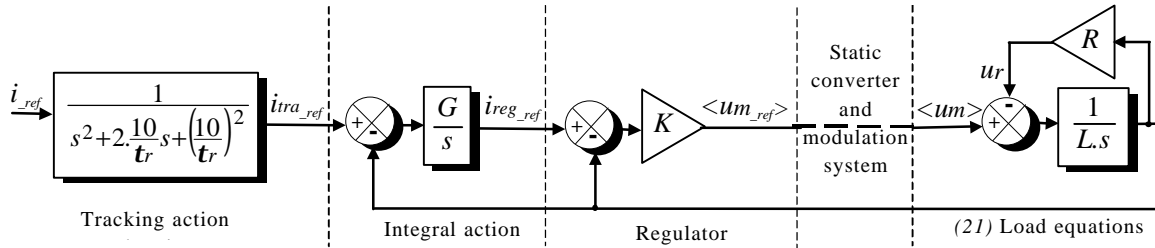


Figure 2 : Input-output modelling of an induction motor

Firstly, in order to suppress the influence of the load (resistor), a rejection action is built by a simple closed loop with a gain  $K$ . Therefore, the resistor voltage is attenuated by this gain as :

$$i(s) = \frac{1}{1 + \frac{L}{K} \cdot s} \cdot i_{reg\_ref}(s) - \frac{1}{1 + \frac{L}{K} \cdot s} \cdot \frac{ur(s)}{K} \quad (1)$$

The maximum value of the current in permanent operating is 30 A. To minimize the influence of the resistor voltage, we must set :

$$\frac{ur(s=0)}{K} < 30 \quad \frac{30 \cdot R}{30} < K$$

As  $R=20\Omega$ , we choose  $K=90$ . With this particular value, we can assume :

$$i(s) = \frac{1}{1 + \frac{L}{K} \cdot s} \cdot i_{reg\_ref}(s)$$

Therefore, a second action is done to get a null static error in permanent error. So, the dynamic behaviour of the system is modelled as :

$$i(s) = \frac{G \cdot K}{L} \cdot \frac{1}{s^2 + \frac{K}{L} \cdot s + \frac{GK}{L}} \cdot i_{ra\_ref}(s) = \frac{G \cdot K}{L} \cdot \frac{1}{s^2 + 2 \cdot z \cdot \omega_n \cdot s + \omega_n^2} \cdot i_{ra\_ref}(s) \quad (1)$$

where  $\omega_n = \sqrt{\frac{GK}{L}}$  and  $z = \frac{1}{2} \sqrt{\frac{K}{L.G}}$ . And, we set  $G = \frac{1-K}{4L.z^2}$  to ensure a slow damping ratio ( $z=3$ ).

Hence, a tracking transfer function is calculated to compensate this dynamic and to set an unity damping with a desirable response time :

$$i(s) = \frac{L}{G.K} \cdot \frac{s^2 + 2.z.\omega_n.s + \omega_n^2}{s^2 + 2.\frac{10}{T_r}.s + \left(\frac{10}{T_r}\right)^2} \cdot \frac{G.K}{L} \cdot \frac{1}{s^2 + 2.z.\omega_n.s + \omega_n^2} \cdot i(s) = \frac{1}{s^2 + 2.\frac{10}{T_r}.s + \left(\frac{10}{T_r}\right)^2} \cdot i(s)$$

### Capacitor voltage balancing (a revoir)

Modulated currents cause unwanted deviations of capacitor voltages. We are going to show that by a right selection of switch patterns we can hold a dc constant value of the capacitor voltage ( $u_{s2}$ ). The switch patterns which are presented fig. 9 (a) and (b) have no effect on the unbalance of the dc link capacitors as capacitors are assumed ideal and the voltage is externally regulated. Whereas, fig. 9 (c) and (d) have the most effect on the balancing because either a positive or a negative current loads the intermediary capacitor ( $C_2$ ) in order to supply the load with an half level voltage. The capacitor  $C_2$  voltage increases in case of (c) and decreases in case (d) as the voltage  $u_s$  is hold constant.

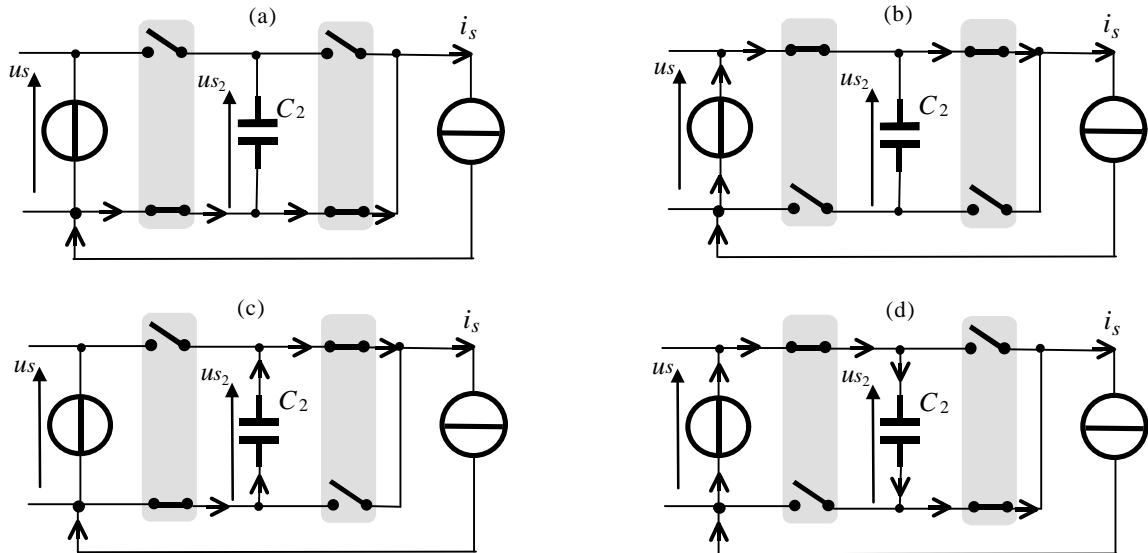


Fig. 9 : Effect of some switch patterns on unbalancing

We can remark that for a wished half level of the modulated voltage, two configurations are possible and will affect the capacitor voltage. The effect of modulated currents onto the load of capacitors is easily deduced. In table 3, we have represented by  $\uparrow$  the voltage increase, by  $\downarrow$  the voltage decrease.

Patterns	$T_1$	$T_2$	$f_1$	$f_2$	$f_3$	$f_4$	$u_m$	$m_1$	$m_2$	$i_{m1}$	$i_{m2}$	$u_{s2}$
2	0	1	0	1	0	0	$u_{s2} \rightarrow \frac{1}{2} . u_s$	0	1	0	$i_s$	$\downarrow$
3	1	0	0	0	1	0	$u_s - u_{s2} \rightarrow \frac{1}{2} . u_s$	1	-1	$i_s$	0	$\uparrow$

Balancing condition

Table 3 : Effect of a half level voltage on the capacitor voltage

So in order to limit the capacitor deviations we have designed a modulation strategy which consists to alternate successfully one loading pattern and one disloading pattern when applying the half

voltage level. Two cases are now considered for the calculation of the durations of electrical conversions.

For small values in the modulated voltage reference, the best choice is to select only voltage half-values because they produce the smallest changes in the current. Two kinds of voltage levels ( $u_s$  and  $u_s/2$ ) and three patterns (No2, No3 and No4 in table 2) will be used to implement the half level modulation. For higher values of the modulated voltage reference, it is preferable to avoid the use of the zero pattern. Thus the full level modulation will be designed by switching among patterns 1, 2 and 3 in table2.

### Full level modulation

A full level modulation occurs when the reference of the modulated voltage is superior to the theoretical half level ( $\langle um_{ref} \rangle > u_s/2$ ). It is implemented by using only the full level and one half level. With a such modulation no zero voltage is applied to the load (fig. 10).

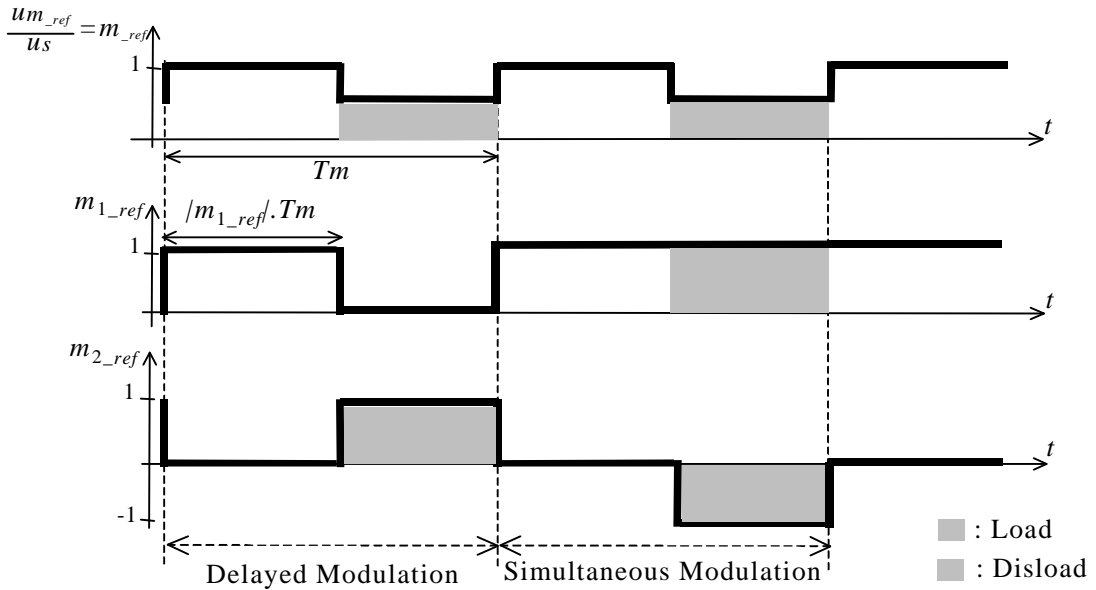


Fig. 10: Effect of the full level modulation onto the capacitor  $C_2$

We recall that the modulated voltage reference is decomposed as a sum of two kinds of conversions : conversion of the full level and conversion of the half level as :

$$\langle um_{ref} \rangle = \langle m_{1\_ref} \rangle \cdot u_s + \langle m_{2\_ref} \rangle \cdot \frac{u_s}{2}$$

We can also write :

$$\frac{\langle um_{ref} \rangle}{u_s} = \langle m_{1\_ref} \rangle + \frac{1}{2} \cdot \langle m_{2\_ref} \rangle$$

If  $u_{s2} < \frac{u_s}{2}$ , the pattern 2 must be chosen to increase the capacitor voltage. In order to assume no zero conversions inside the modulation period, a delayed modulation of the two conversion functions must be implemented and, so, the following constraint must be satisfied :

$$|\langle m_{1\_ref} \rangle| + |\langle m_{2\_ref} \rangle| = 1$$

As the variation domain of conversion functions is binary, this constraint yields to

$$\langle m_{1\_ref} \rangle + \langle m_{2\_ref} \rangle = 1$$

By taking into account this constraint into the preceding equation, we get :

$$\langle m_{1\_ref} \rangle = 2 \cdot \frac{\langle um_{ref} \rangle}{us} - 1 \quad \text{and} \quad \langle m_{2\_ref} \rangle = 2 - 2 \cdot \frac{\langle um_{ref} \rangle}{us}$$

If  $us_2 > \frac{us}{2}$ , the pattern 3 is chosen to decrease the capacitor voltage. A simultaneous modulation of both conversion functions is implemented by setting :

$$\langle m_{1\_ref} \rangle = 1 \quad \text{and} \quad \langle m_{2\_ref} \rangle = 2 \left( \frac{\langle um_{ref} \rangle}{us} - 1 \right)$$

### Half level modulation

If  $us_2 < \frac{us}{2}$ , we need only the half level as shown on fig. 11.

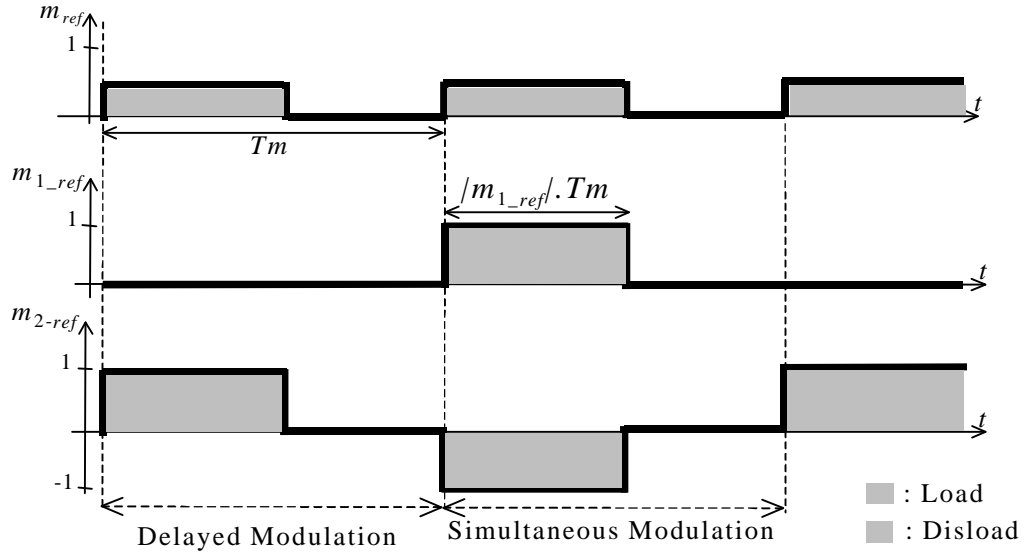


Fig. 11: Effect of the half level modulation onto the capacitor  $C_2$

The pattern 2 will be chosen in order to increase the capacitor voltage. Therefore we get :

$$\langle m_{1\_ref} \rangle = 0 \quad \text{and} \quad \langle m_{2\_ref} \rangle = 2 \cdot \frac{\langle um_{ref} \rangle}{us}$$

Otherwise, the pattern 1 is chosen in order to decrease the capacitor voltage and a simultaneous modulation is used. In this case, conversion functions have different signs but have the same modulus :

$$\langle m_{1\_ref} \rangle = -\frac{1}{2} |\langle m_{2\_ref} \rangle|$$

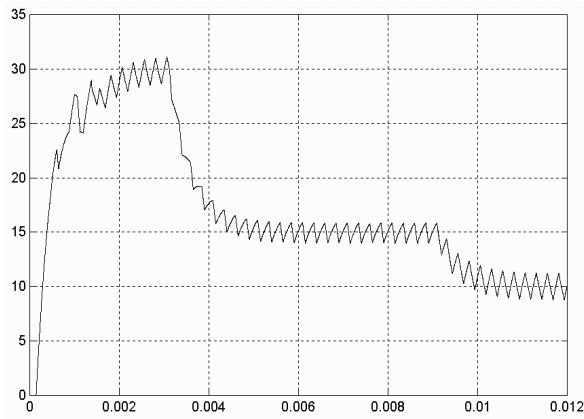
By taking into account this constraint into the preceding equation, we get :

$$\langle m_{1\_ref} \rangle = 2 \cdot \frac{\langle um_{ref} \rangle}{us} \quad \text{and} \quad \langle m_{2\_ref} \rangle = -2 \cdot \frac{\langle um_{ref} \rangle}{us}$$

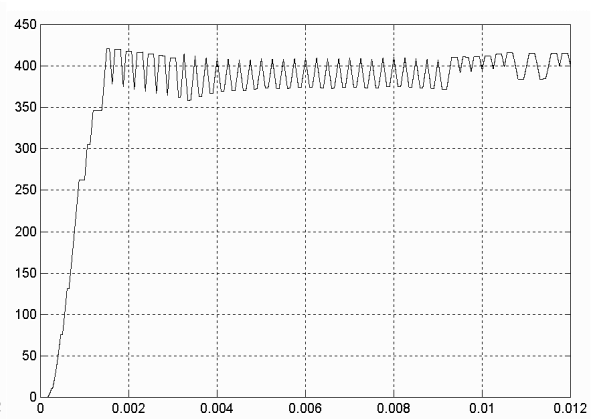
Effect on the capacitor voltage	$\langle um_{ref} \rangle > \frac{us}{2}$	$\langle um_{ref} \rangle < \frac{us}{2}$
Decrease	$\langle m_{1\_ref} \rangle = 1$ $\langle m_{2\_ref} \rangle = 2 \left( \frac{\langle um_{ref} \rangle}{us} - 1 \right)$	$\langle m_{1\_ref} \rangle = 2 \left( \frac{\langle um_{ref} \rangle}{us} \right)$ $\langle m_{2\_ref} \rangle = -2 \left( \frac{\langle um_{ref} \rangle}{us} \right)$
Increase	$\langle m_{1\_ref} \rangle = 2 \cdot \frac{\langle um_{ref} \rangle}{us} - 1$ $\langle m_{2\_ref} \rangle = 2 - 2 \cdot \frac{\langle um_{ref} \rangle}{us}$	$\langle m_{1\_ref} \rangle = 0$ $\langle m_{2\_ref} \rangle = 2 \left( \frac{\langle um_{ref} \rangle}{us} \right)$

Table 4 : Evaluation of rules for full and half level modulation

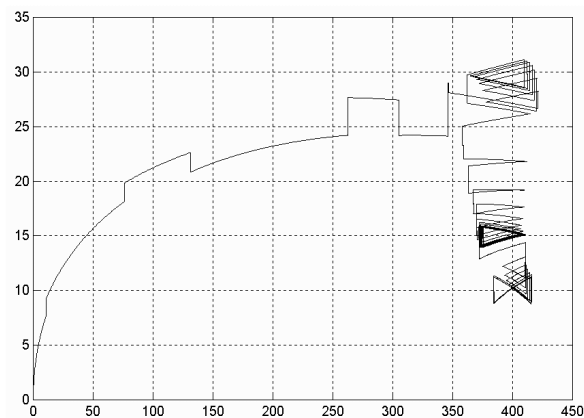
## 5. SIMULATION RESULTS



Courant dans la charge en Ampère ( $i_s$ )



Tension aux bornes du condensateur ( $usc_2$ )



Plan de phase

Joli ce cycle, non ?

Bon, le problème c'est la trop grande largeur en régime permanent due à l'excursion trop importante de la tension capa. Mais, ce n'est en fait qu'une commande très simple (sans capteur de tension !) et ces formes d'onde vont me permettre en fait d'avoir une référence pour faire mieux.

Je suis d 'ailleurs en train d'en mettre au point une autre commande qui tiens compte de l'information de la tension. Mais cela sera pour un autre article...

## CONCLUSION

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