Digital Predictive Current Control of a Three-Phase Four-Leg Inverter

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***Abstract*—While the classical control techniques for three-phase two-level four-leg inverters are based on pulse width modulation or three-dimensional space vector modulation, this paper presents a simple digital current control strategy without the modulation stage. The proposed controller uses the discrete nature of the four-leg inverter and filter to generate the switching states. By using a predictive cost function, the optimal switching state to be applied in the next sampling interval is selected. The proposed controller offers excellent reference tracking with less current harmonic distortion for balanced and unbalanced loading conditions. The feasibility of the proposed strategy is verified by digital implementation on a dSPACE DS1104-based rapid prototype platform.**

***Index Terms*—Control systems, Current control, DC-AC power conversion, Digital control, Discrete time signals, Finite-set model predictive control, Four-leg inverters**

NOMENCLATURE

$\mathbf{A}, \mathbf{B}, \mathbf{C}$	Parameters matrix dimension 3x3
$\mathbf{F}, \mathbf{G}$	Parameters matrix dimension 3x3
$\mathbf{x}$	State variables vector
$\mathbf{u}$	Input variables vector
$\mathbf{y}$	Output variables vector
$\mathbf{i}$	Load current vector $[i_u \ i_v \ i_w]^T$
$\mathbf{v}$	Load voltage vector $[v_{ux} \ v_{vx} \ v_{wx}]^T$
$\mathbf{i}^*$	Reference current vector $[i_u^* \ i_v^* \ i_w^*]^T$
x_k	k^{th} state variable
$\dot{x}_k$	k^{th} state variable derivative
a_k	k^{th} coefficient of $\mathbf{A}$
b_k	k^{th} coefficient of $\mathbf{B}$
v_{dc}	DC-link voltage
i_j	Current in leg $j = u, v, w, x$
S_j	Switching state of leg $j = u, v, w, x$
R_{fj}	Filter resistance of leg $j = u, v, w, x$
L_{fj}	Filter inductance of leg $j = u, v, w, x$
R_j	Load resistance of leg $j = u, v, w, x$
T_s	Sampling time

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I. INTRODUCTION

The four-leg converter is very flexible and widely demanded for three-phase four-wire power electronics applications including the following: distributed generation (DG) [1], [2] with grid-connected [3], [4] or stand-alone operation [5] to deliver high quality power supply to the arbitrary consumer loads; shunt active power filters also known as DSTATCOM [6] to compensate non-linear load harmonics, imbalances, and reactive power in order to maintain sinusoidal supply currents; series active power filters also known as dynamic voltage restorers (DVR) [7] to provide voltage support to sensitive loads during voltage sags, swells, and imbalances; unified power quality conditioners (UPQC) [8] to perform DSTATCOM and DVR functions simultaneously; static Var compensators (SVC) [9] to improve the system's power factor and voltage stability; grid power quality enhancement [10]; active front end (AFE) rectifiers [11] to deal with line imbalances and fault-tolerant operation; common-mode active filters [12] for the minimization of common-mode voltage and electromagnetic interference (EMI); electric motor drive applications for electric vehicles [13] such as independent control of two or more motors from an inverter [14], fault tolerant operation of drives [15], and control of two-phase motors [16]; uninterruptible power supplies (UPS) [17] to feed unbalanced loads with less harmonic current distortion; rural electrification schemes; aircraft power supply networks; satellite earth stations; military, medical and telecommunication equipment.

The linear current control techniques use PID regulators to eliminate steady-state current errors and a modulation state to generate gating signals for the four-leg inverters [18]. The poor performance of the PI controller with grid harmonics, together with the switching dead time and control delay time cause poor output current quality for grid-connected inverters [19]. Various carrier-less modulation schemes (such as hysteresis, flux vector [20] and selective harmonic elimination (SHE) [21]), carried-based sinusoidal pulse width modulation (SPWM) [22], and three-dimensional space vector modulation (3D-SVM) [11], [18] methods have been used for the four-leg converters. The calculation of switching angles and their digital implementation for SHE is quite complex. Compared to the SPWM, 3D-SVM offers many advantages including good DC-link utilization, lower switching frequency and minimal output distortion [11], [23], [24].

On the other hand, the cost-function based finite control set model predictive control (FCS-MPC) has found recent

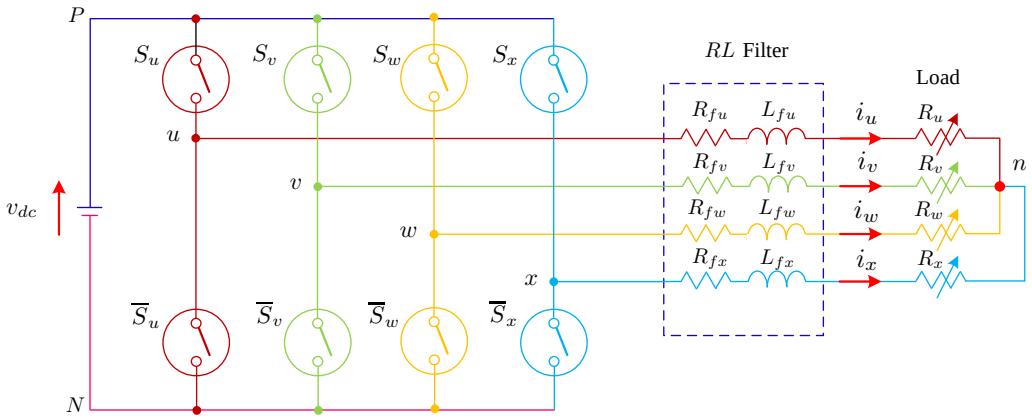

Figure 1. Three-phase two-level four-leg inverter topology.

application in power electronics [25]. This method is an attractive alternative to the classical control methods, due to its simple concept, fast dynamic response, and the easy inclusion of nonlinearities and constraints in the controller design [26]. Moreover, this scheme does not require internal current control loops and modulators, which greatly reduces its complexity. This digital control technique has successfully been applied to a wide range of power converters, drives and energy system applications [27]–[31].

In this paper, the concept of FCS-MPC has been extended for digital current control of three-phase two-level four-leg inverters. This control scheme predicts the future load current behavior for each valid switching state of the converter, in terms of the measured load current and predicted load voltage. The predictions are evaluated with a cost function that minimizes the error between the predicted currents and their references at the end of each sampling time.

To validate the proposed method, different cases are verified through experimental setups based on the dSPACE DS1104 rapid prototyping controller.

This paper is organized as follows: in section II, the mathematical model of the converter-load system is presented, followed by the explanation of the proposed control strategy in section III. In section IV, practical considerations and experimental results are presented. Finally, in section V appropriate conclusions are drawn.

II. Four-Leg Inverter Model

A. Topology

The power converter topology for a four-leg inverter with output RL filter is shown in Fig. 1. The R_f represents the leakage resistance of the filter. The neutral inductance L_{fx} helps in reducing the neutral-leg switching frequency ripple [11]. The fourth leg is connected to the neutral point of the load through the RL filter, allowing for controllability of the zero sequence current/voltage. The additional fourth leg increases the number of gating signals and thus the control complexity compared to the three-leg inverter. However, it can handle single-phase or three-phase, balanced or unbalanced, linear or non-linear loads without affecting the DC-link capacitor life.

B. Mathematical Model of the System

The four control signals named S_u, S_v, S_w and S_x form a total of 16 (2^4) switching states of the converter. The voltages in each leg of the inverter, measured from the negative point of the DC-link (N) can be expressed as,

$$\begin{bmatrix} v_{uN} \\ v_{vN} \\ v_{wN} \\ v_{xN} \end{bmatrix} = \begin{bmatrix} S_u \\ S_v \\ S_w \\ S_x \end{bmatrix} v_{dc}, \tag{1}$$

which can be re-written as:

$$v_{jN} = S_j v_{dc}, \quad j = u,\ v,\ w,\ x. \tag{2}$$

The voltage applied to the output RL filter, in terms of these voltages, is:

$$\begin{bmatrix} v_{ux} \\ v_{vx} \\ v_{wx} \end{bmatrix} = \begin{bmatrix} S_u - S_x \\ S_v - S_x \\ S_w - S_x \end{bmatrix} v_{dc}. \tag{3}$$

The above expression can be simplified to:

$$v_{yx} = v_{yN} - v_{xN} = (S_y - S_x) v_{dc}, \quad y = u,\ v,\ w. \tag{4}$$

The inverter voltages are given as,

$$\begin{aligned} \begin{bmatrix} v_{uN} \\ v_{vN} \\ v_{wN} \\ v_{xN} \end{bmatrix} &= \begin{bmatrix} R_{fu} & 0 & 0 & 0 \\ 0 & R_{fv} & 0 & 0 \\ 0 & 0 & R_{fw} & 0 \\ 0 & 0 & 0 & R_{fx} \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \\ i_x \end{bmatrix} \\ &+ \begin{bmatrix} L_{fu} & 0 & 0 & 0 \\ 0 & L_{fv} & 0 & 0 \\ 0 & 0 & L_{fw} & 0 \\ 0 & 0 & 0 & L_{fx} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_u \\ i_v \\ i_w \\ i_x \end{bmatrix} \\ &+ \begin{bmatrix} R_u & 0 & 0 & 0 \\ 0 & R_v & 0 & 0 \\ 0 & 0 & R_w & 0 \\ 0 & 0 & 0 & R_x \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \\ i_x \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} v_{nN}, \end{aligned} \tag{5}$$

which can be re-written as:

$$v_{jN} = (R_{fj} + R_j) i_j + L_{fj} \frac{di_j}{dt} + v_{nN}, \quad j = u,\ v,\ w,\ x. \tag{6}$$

The derivative of the output current vector can be obtained from (6), as follows:

$$\frac{di_j}{dt} = \frac{1}{L_{fj}}\left[(v_{jN} - v_{nN}) - (R_{fj} + R_j)i_j\right], \quad j = u,\ v,\ w,\ x. \tag{7}$$

Based on (2) and (6), the load neutral voltage v_{nN} can be expressed as follows:

$$v_{nN} = L_{eq}v_{dc}\sum_{k=u,v,w,x}\frac{S_k}{L_{fk}} - L_{eq}\sum_{k=u,v,w,x}\frac{R_{fk}+R_k}{L_{fk}}i_k, \tag{8}$$

with,

$$L_{eq} = \left(\frac{1}{L_{fu}} + \frac{1}{L_{fv}} + \frac{1}{L_{fw}} + \frac{1}{L_{fx}}\right)^{-1}, \tag{9}$$

and,

$$i_u + i_v + i_w + i_x = 0. \tag{10}$$

The system in (6) can be represented in space-state form as:

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u},\\ \mathbf{y} &= \mathbf{C}\mathbf{x},\end{aligned} \tag{11}$$

with,

$$\begin{aligned}\mathbf{x} &= \begin{bmatrix} x_1 & x_2 & x_3 \end{bmatrix}^T = \begin{bmatrix} i_u & i_v & i_w \end{bmatrix}^T,\\ \mathbf{u} &= \begin{bmatrix} u_1 & u_2 & u_3 \end{bmatrix}^T = \begin{bmatrix} v_{ux} & v_{vx} & v_{wx} \end{bmatrix}^T.\end{aligned} \tag{12}$$

The block diagram of the system in (11) is shown in Fig. 2. The matrix $\mathbf{A}$ is given by:

$$\mathbf{A} = \begin{bmatrix} a_1 & a_2 & a_3\\ a_4 & a_5 & a_6\\ a_7 & a_8 & a_9 \end{bmatrix}, \tag{13}$$

where the coefficients a_i, $i = 1, ..., 9$ are given as follows:

$$\begin{aligned}
a_1 &= -\frac{R_{fu}+R_u}{L_{fu}} + \frac{L_{eq}}{L_{fu}}\left(\frac{R_{fu}+R_u}{L_{fu}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_2 &= \frac{L_{eq}}{L_{fu}}\left(\frac{R_{fv}+R_v}{L_{fv}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_3 &= \frac{L_{eq}}{L_{fu}}\left(\frac{R_{fw}+R_w}{L_{fw}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_4 &= \frac{L_{eq}}{L_{fv}}\left(\frac{R_{fu}+R_u}{L_{fu}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_5 &= -\frac{R_{fv}+R_v}{L_{fv}} + \frac{L_{eq}}{L_{fv}}\left(\frac{R_{fv}+R_v}{L_{fv}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_6 &= \frac{L_{eq}}{L_{fv}}\left(\frac{R_{fw}+R_w}{L_{fw}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_7 &= \frac{L_{eq}}{L_{fw}}\left(\frac{R_{fu}+R_u}{L_{fu}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_8 &= \frac{L_{eq}}{L_{fw}}\left(\frac{R_{fv}+R_v}{L_{fv}} - \frac{R_{fx}+R_x}{L_{fx}}\right),\\
a_9 &= -\frac{R_{fw}+R_w}{L_{fw}} + \frac{L_{eq}}{L_{fw}}\left(\frac{R_{fw}+R_w}{L_{fw}} - \frac{R_{fx}+R_x}{L_{fx}}\right).
\end{aligned} \tag{14}$$

The matrix $\mathbf{B}$ is given by:

$$\mathbf{B} = \begin{bmatrix} b_1 & b_2 & b_3\\ b_4 & b_5 & b_6\\ b_7 & b_8 & b_9 \end{bmatrix}, \tag{15}$$

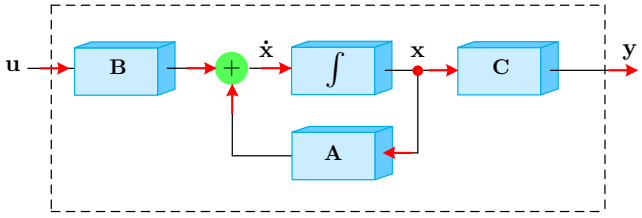

Figure 2. Block diagram of the system in state variables.

where the coefficients b_i, $i = 1, ..., 9$, are defined as:

$$\begin{aligned}
b_1 &= \frac{v_{dc}}{L_{fu}}\left(1 - \frac{L_{eq}}{L_{fu}}\right),\\
b_2 &= -\frac{v_{dc}}{L_{fu}}\frac{L_{eq}}{L_{fv}},\\
b_3 &= -\frac{v_{dc}}{L_{fu}}\frac{L_{eq}}{L_{fw}},\\
b_4 &= -\frac{v_{dc}}{L_{fv}}\frac{L_{eq}}{L_{fu}},\\
b_5 &= \frac{v_{dc}}{L_{fv}}\left(1 - \frac{L_{eq}}{L_{fv}}\right),\\
b_6 &= -\frac{v_{dc}}{L_{fv}}\frac{L_{eq}}{L_{fw}},\\
b_7 &= -\frac{v_{dc}}{L_{fw}}\frac{L_{eq}}{L_{fu}},\\
b_8 &= -\frac{v_{dc}}{L_{fw}}\frac{L_{eq}}{L_{fv}},\\
b_9 &= \frac{v_{dc}}{L_{fw}}\left(1 - \frac{L_{eq}}{L_{fw}}\right).
\end{aligned} \tag{16}$$

Matrix $\mathbf{C}$ is defined as:

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1 \end{bmatrix}. \tag{17}$$

III. Digital Predictive Current Control

The simplified structure of the proposed digital predictive current control scheme is shown in Fig. 3. This control scheme is basically an optimization algorithm and thus it has to be implemented digitally in microprocessor-based hardware. Consequently, the analysis has to be developed using discrete mathematics in order to consider additional restrictions such as delays and approximations, etc. [25]. Predictive control is characterized by its use of the system model to predict the behavior of the variables to be controlled. The controller uses this information to obtain the optimal actuation, according to a predefined optimization criterion. Furthermore, the predictive control algorithm is very easy and intuitive to understand consisting of the following three main steps:

1) References and Measurements: The control objectives are obtained and the variables necessary for the prediction model are measured and calculated. In this case, the measurements of output currents and DC-link voltage are obtained and the future load current reference can be calculated using the fourth order Lagrange extrapolation as follows [32]:

$$\mathbf{i}^*[k+1] = 4\,\mathbf{i}^*[k] - 6\,\mathbf{i}^*[k-1] + 4\,\mathbf{i}^*[k-2] - \mathbf{i}^*[k-3], \tag{18}$$

The above method can be used for a wide range of frequencies of $\mathbf{i}^*$. No extrapolation is required when sampling time T_s is small enough.

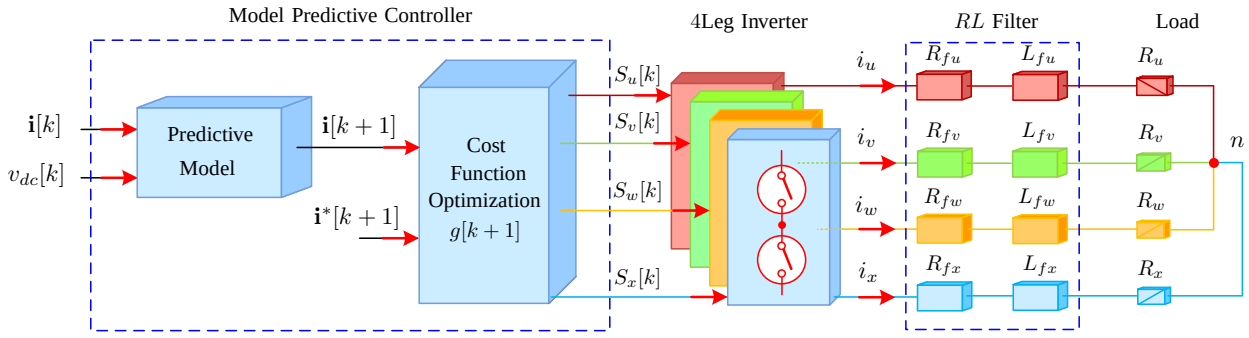

Figure 3. Proposed predictive digital current control scheme.

2) Prediction Model: As a second consideration, it is important to obtain the converter-load system model for the load current prediction. Since the controller operates in discrete time, both the controller and the system model need to be represented in a discrete time domain [25]. The discrete time model consists of a recursive matrix equation that allows the system prediction. This means, for a given sampling time T_s, it is possible to predict the system states at any instant $(k+1)T_s$, with the knowledge of system states and control variables at instant $(k)T_s$. Based on (11), the recursive equation of the system represented in Fig. 1 is given by:

$$\mathbf{i}[k+n+1] = \mathbf{F}\mathbf{i}[k+n] + \mathbf{G}\mathbf{u}[k+n], \quad n = 0, 1, 2..... \tag{19}$$

where,

$$\begin{aligned} \mathbf{F} &= \begin{bmatrix} f_1 & f_2 & f_3 \\ f_4 & f_5 & f_6 \\ f_7 & f_8 & f_9 \end{bmatrix} = e^{\mathbf{A}T_s}, \\ \mathbf{G} &= \begin{bmatrix} g_1 & g_2 & g_3 \\ g_4 & g_5 & g_6 \\ g_7 & g_8 & g_9 \end{bmatrix} = \mathbf{A}^{-1}\left(\mathbf{F} - \mathbf{I_{3x3}}\right)\mathbf{B}. \end{aligned} \tag{20}$$

$\mathbf{I_{3x3}}$ is the identity matrix. Since the matrices $\mathbf{A}$ and $\mathbf{B}$ are of 3x3 size, the calculation of matrices $\mathbf{F}$ and $\mathbf{G}$ is complex. But, the calculation of these matrices can be performed offline with the aid of mathematical computing tools such as MATLAB. The system in (19) consists of two components:

- a free response component $\mathbf{i_f}$, given by:

$$\mathbf{i_f}[k+1] = \mathbf{F}\,\mathbf{i}[k], \tag{21}$$

- and a forced response component $\mathbf{i_s}$ (control component), defined as:

$$\mathbf{i_s}[k+1] = \mathbf{G}\,\mathbf{u}[k]. \tag{22}$$

As shown in Fig. 3, the output current predictions require the load current and voltage (which is a function of the switching signals and the DC-link voltage) values. The algorithm calculates all 16 possible conditions that the state variables can achieve.

3) Cost Function Optimization: As a final stage, the predicted values are used to evaluate a cost function which deals with the control objective. To choose the optimal switching state to be applied to the inverter, the 16 predictions obtained for $\mathbf{i}[k+1]$ are compared with their references using a cost function g as follows:

$$\begin{aligned} g[k+1] &= ||\mathbf{i}^*[k+1] - \mathbf{i}[k+1]||^2 \\ &= \left(i_u^*[k+1] - i_u[k+1]\right)^2 \\ &+ \left(i_v^*[k+1] - i_v[k+1]\right)^2 \\ &+ \left(i_w^*[k+1] - i_w[k+1]\right)^2. \end{aligned} \tag{23}$$

The output current equals its reference when $g = 0$. Therefore, the optimization goal of the cost function is to achieve a near-zero g value. The voltage vector that minimizes the cost function is chosen and then applied at the next sampling instant. During each sampling instant, the minimum value of g is selected from the 16 function values. The algorithm selects a switching state which produces this minimal value and then applies it during the whole $(k+1)$ period.

IV. Experimental Results

A. Rapid Prototype Platform

To validate the proposed digital control method, experimental results have been obtained using a three-phase two-level four-leg inverter prototype with the parameters as indicated in Table I of Appendix.

The prototype is a Semikron IGBT Power Electronics Teaching System with a SKD51/14 rectifier and SKM50GB123D IGBT modules. The drivers are based on three SKHI22A-R dual cores which are powered with 0/15V 160mA supply. The control algorithm has been implemented using MATLAB-Simulink in a Real-Time Interface (RTI) on the dSPACE DS1104 R&D controller board. Three current sensors LEMLA55-P and one DC-link voltage sensor LV25-600 are used and their analog values are supplied to a DS1104 CLP board. This CLP board converts these analog values to digital for use with the predictive control algorithm running on a host personnel computer. Digital outputs from the DS1104 CLP board are used to deliver the gate drive signals for the IGBTs. These outputs are set directly by the control algorithm, and no modulator is needed.

B. Delay Compensation

The predictive control algorithm can be implemented in the $(k+1)$ state when verifying it through MATLAB simulations.

But in the experimental verification, the delay produced by the digital signal processor, gate drivers and switching devices is inevitable. Out of all these the delay produced by the digital signal processor is most significant and it must be compensated. The delays associated with the response of the gate drive circuitry and switching of the devices can be neglected, due to their small magnitude, even for high sampling rates. This delay can easily be compensated by calculating the cost function at the end of the next sampling period, i.e. $g[k+2]$. Thus, the selected switching state can be applied at instant $(k+1)$, and therefore one sampling period is available for calculations. The aforementioned compensation requires the calculation of $\mathbf{i}[k+1]$ and $\mathbf{v}[k+1]$ in order to obtain the basis for the calculation of $g[k+2]$. These terms are obtained from eq. (2) and eq. (19) and the switching state S_j $(j = u, v, w, x)$, selected in the previous iteration [33].

C. Control Algorithm

The predictive algorithm has been implemented in a very simple way using the MATLAB S-builder function block as indicated in the code. This block operates with a discrete update method at the sample time defined for the predictive algorithm (T_s). The first three lines of the code declare the extrapolated reference currents i_u^*, i_v^* and i_w^* in $(k+2)$, which are defined by the user. Lines 4 to 6, correspond to the measurement of load currents i_u, i_v and i_w, respectively. Line 7 is the measurement of the DC-link voltage v_{dc}. In order to compensate the delay, the load current prediction in $(k+1)$ has been performed between lines 10 to 15 using the measured load currents and the optimal load voltages. The optimum load voltage is obtained using the optimal switching states in the previous iteration and the DC-link voltage. Lines 17 to 39 correspond to the predictive algorithm. From lines 20 to 22, load voltage estimation in $(k+1)$ is performed using the 16 possible switching states. As shown in lines 24 to 29, the load voltages and currents in $(k+1)$ are used to predict the load currents in $(k+2)$. With this approach the most significant delay caused by the digital signal processor can be compensated.

The constants $f1$ to $f9$ and $g1$ to $g9$ are defined in eq. (20). These constants can be calculated off-line and should be predefined in the initialization file. The load current predictions in $(k+2)$ are compared with their respective references as indicated in lines 31 to 33, which are merged into a cost function g in line 34. The optimization for cost function has been implemented between lines 35 to 38. In lines 41 to 43, the values of the optimal output voltages are considered in order to be used in the next sampling time. Finally, the optimal switching state that minimizes the cost function g is applied as an output of the predictive algorithm as shown in lines 45 to 48. This algorithm is summarized in the flow chart indicated in Fig. 4.

```
1
2  iu_ref = in[0];
3  iv_ref = in[1];
4  iw_ref = in[2];
5  iu = in[3];
6  iv = in[4];
7  iw = in[5];
8  vdc = in[6];
9  % delay compensation
10 % current prediction in k+1
11 iuk1[i][0] = f1*iu + f2*iv + f3*iw +
12              g1*vux_opt + g2*vvx_opt + g3*vwx_opt;
13 ivk1[i][1] = f4*iu + f5*iv + f6*iw +
14              g4*vux_opt + g5*vvx_opt + g6*vwx_opt;
15 iwk1[i][2] = f7*iu + f8*iv + f9*iw +
16              g7*vux_opt + g8*vvx_opt + g9*vwx_opt;
17 % predictive algorithm
18 index_s_min=1;
19 g_min = 2e20;
20 for i=0:15
21    vux[i] = (S[i][0]-S[i][3])*vdc;
22    vvx[i] = (S[i][1]-S[i][3])*vdc;
23    vwx[i] = (S[i][2]-S[i][3])*vdc;
24    % current prediction in k+2
25    iuk2[i][0] = f1*iuk1 + f2*ivk1 + f3*iwk1 +
26                 g1*vux + g2*vvx + g3*vwx;
27    ivk2[i][1] = f4*iuk1 + f5*ivk1 + f6*iwk1 +
28                 g4*vux + g5*vvx + g6*vwx;
29    iwk2[i][2] = f7*iuk1 + f8*ivk1 + f9*iwk1 +
30                 g7*vux + g8*vvx + g9*vwx;
31    % cost function
32    aux1 = (iu_ref-iuk2[i][0])*(iu_ref-iuk2[i][0]);
33    aux2 = (iv_ref-ivk2[i][1])*(iv_ref-ivk2[i][1]);
34    aux3 = (iw_ref-iwk2[i][2])*(iw_ref-iwk2[i][2]);
35    g = aux1 + aux2 + aux3;
36    if g<g_min),
37         index_s_min = i;
38         g_min = g;
39    end
40 end
41 % for delay compensation
42 vux_opt = vux[index_s_min];
43 vvx_opt = vvx[index_s_min];
44 vwx_opt = vwx[index_s_min];
45 % output
46 Su = S[index_s_min][0];
47 Sv = S[index_s_min][1];
48 Sw = S[index_s_min][2];
49 Sx = S[index_s_min][3];
```

D. Experimental Results

To demonstrate the effectiveness of the proposed digital predictive current control strategy, experimental results with balanced and unbalanced loads are presented during steady-state and transient-state. The results for the following four cases are developed for balanced loading conditions (R_u = R_v = R_w = 2.5Ω), and they are presented in Figs. 5 to 8:

- Case-1: balanced references:
  I_u^* = I_v^* = I_w^* = 10A, f_u^* = f_v^* = f_w^* = 50Hz,
- Case-2: unbalanced references:
  I_u^* = 10A, I_v^* = I_w^* = 5A, f_u^* = f_v^* = 50Hz, f_w^* = 100Hz,
- Case-3: step change in balanced references:
  I_u^* = I_v^* = I_w^* = 0 to 10A, f_u^* = f_v^* = f_w^* = 50Hz,
- Case-4: step change in unbalanced references:
  I_u^* = 0 to 10A, I_v^* = 0 to 5A, I_w^* = 0 to 7A, f_u^* = f_w^* = 50Hz, f_v^* = 100Hz.

In Case-5 to Case-8, the above four cases are repeated for unbalanced loading conditions. The unbalance in loads is provided as, R_u = 2.5Ω, R_v = R_w = 5Ω, L_{fu} = L_{fv} = L_{fx} = $12mH$, L_{fw} = $6mH$. The variation in L_{fw} represents

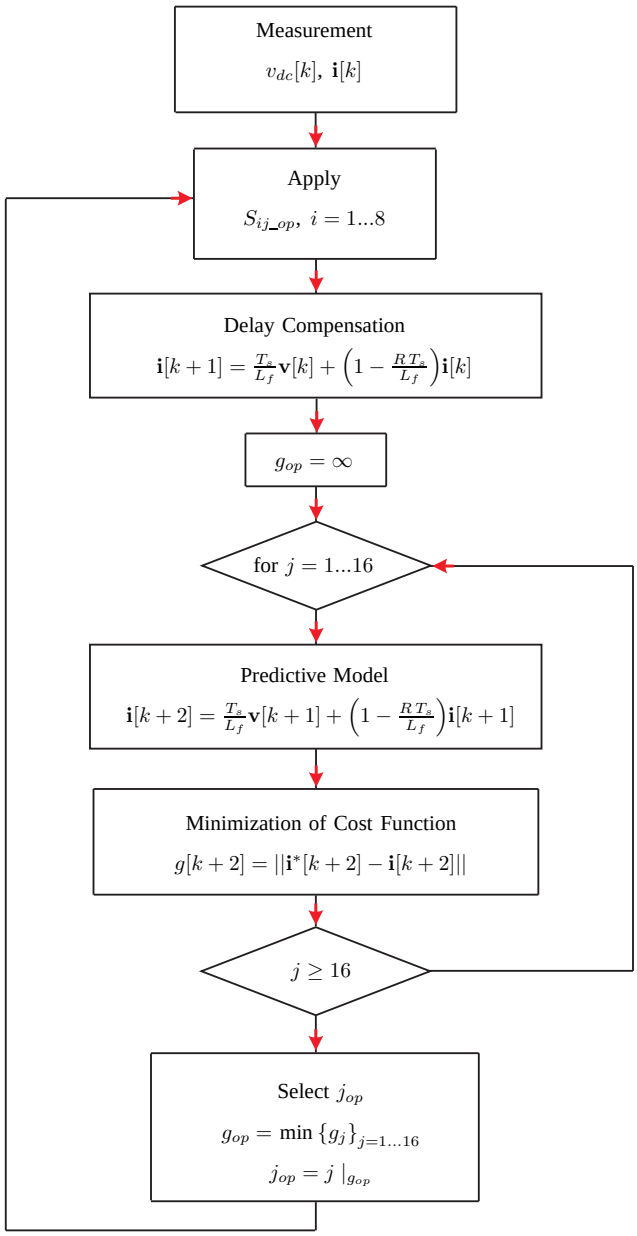

Figure 4. Flow chart of the predictive current control algorithm.

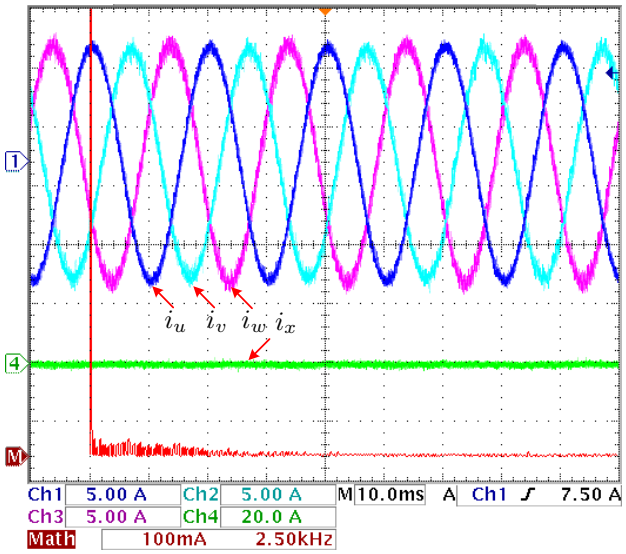

Figure 5. Results for Case-1 – balanced loads with balanced reference currents.

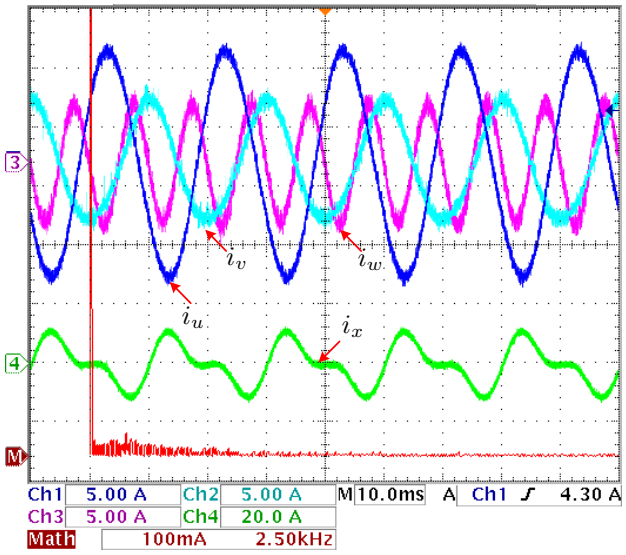

Figure 6. Results for Case-2 – balanced loads with unbalanced reference currents.

the changes in filter parameters. The information about filter and load parameter variation is not provided to the digital predictive current controller.

The Case-1 results are shown in Fig. 5 in steady-state. Since the references are balanced, the load currents are observed to be balanced with an amplitude of 10A and a frequency of 50Hz. Since the load currents are balanced, the neutral current (i_x=$-i_u-i_v-i_w$) is observed to be zero. The frequency spectrum of the load current i_u is spread over the entire frequency range, because this method does not have a fixed switching frequency. But, the magnitude of the low order harmonics is observed to be very small compared to the fundamental harmonic, as shown in FFT of Fig. 5. These low harmonic frequencies are due to the use of an autotransformer connection feeding a three-phase rectifier connected to the AC source side. This connection leads to a contaminated DC-link source for the experimental prototype. In this case, a Total Harmonic Distortion (THD) of 4.61%, 5.72% and 5.81% for currents i_u, i_v and i_w was observed, respectively. It is expected that with a clean AC supply, the THD can be reduced.

The Case-2 results, as shown in Fig. 6, reveal balanced loads and unbalanced references in steady-state. This is the typical situation where the independent single-phase loads with different amplitudes and frequencies are connected to the four-leg inverter.

The four-leg inverter generates independent voltages on each leg and thus helps in controlling zero sequence voltage/current. The load currents track their references very well. The amplitudes of currents in phases u, v and w are observed to be 10A, 5A and 5A, respectively. Due to the unbalanced load currents, the neutral current flows through the fourth leg.

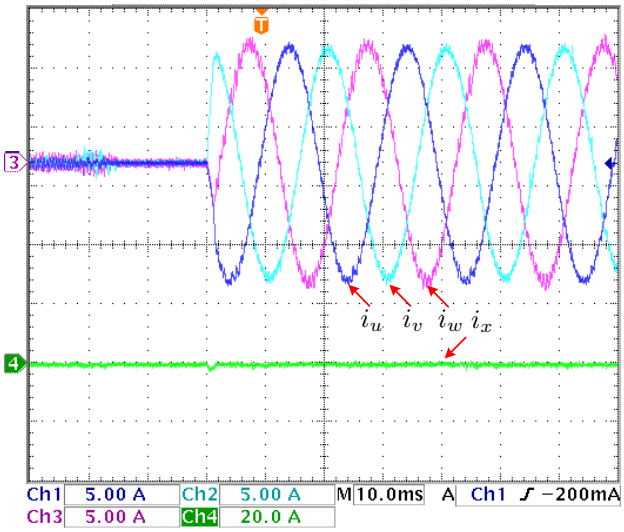

Figure 7. Results for Case-3 – balanced loads with step change in balanced reference currents.

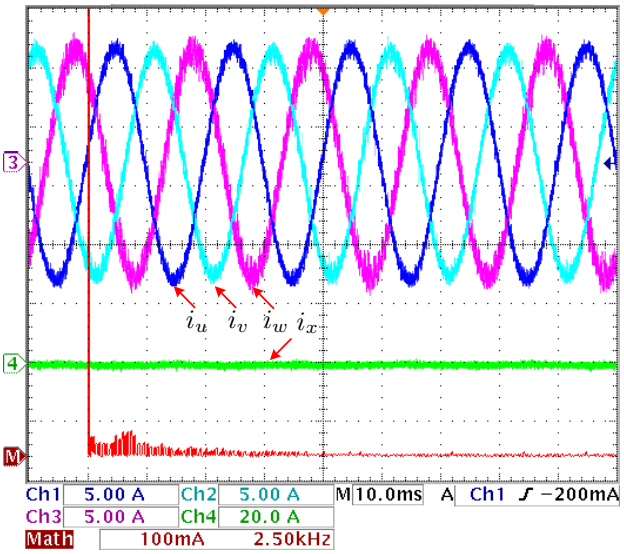

Figure 9. Results for Case-5 – unbalanced loads with balanced reference currents.

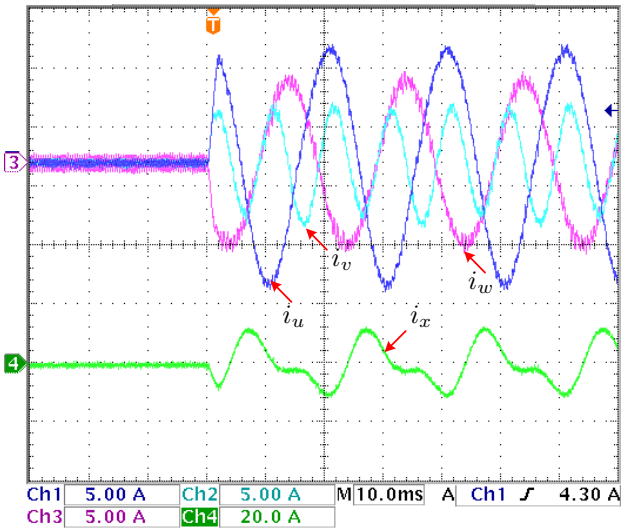

Figure 8. Results for Case-4 – balanced loads with step change in unbalanced reference currents.

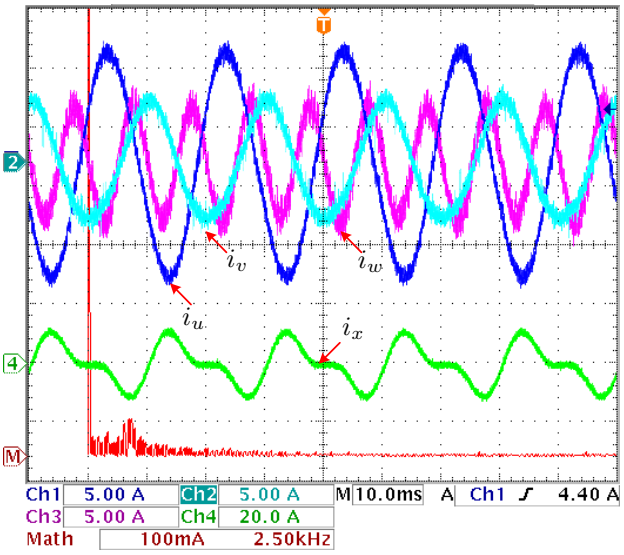

Figure 10. Results for Case-6 – unbalanced loads with unbalanced reference currents.

The neutral current is not sinusoidal as the frequencies of three phases u, v and w are different. For the load current i_u spectrum, the magnitude of the low order harmonics as shown in FFT of Fig. 6 is observed to be very small, similar to the magnitude in Case-1. A THD of 6.03%, 11.50% and 13.05% for currents i_u, i_v and i_w, respectively, was observed. In this case, a higher THD value was observed in phases with small current amplitudes. It is expected that with higher current values and with a clean AC supply, the THD values can decrease. The transient operation with step-change in loads from 0A to Case-1 and Case-2 are presented in Figs. 7 and 8, respectively. The dynamic response of the load currents is observed to be very fast with no overshoot in either case. This dynamic response has been achieved without any penalty in the reference tracking. The proposed controller is very robust and uses no internal current control loops or PI regulators.

The Case-5 results, with unbalanced loads and balanced references in steady-state, are presented in Fig. 9. Similar to Case-1, the load currents are observed to be balanced with an amplitude of 10A and frequency of 50Hz, despite the unbalance in the load and filter parameters. It is important to note that the variations in load and filter parameters are not provided to the digital current controller. The controller generates a switching state which produces less error between the references and predicted load currents.

From this case, it is evident that the controller is very robust, withstanding the load parameter variations. The magnitude of the low order harmonics for load current i_u are comparable to Case-1. The main differences between Case-1 and Case-5 are given by the THD current and the ripple observed. In this case, our experimental results presented a THD of 5.17%, 6.38% and 9.39% for currents i_u, i_v and i_w, respectively. The Case-6

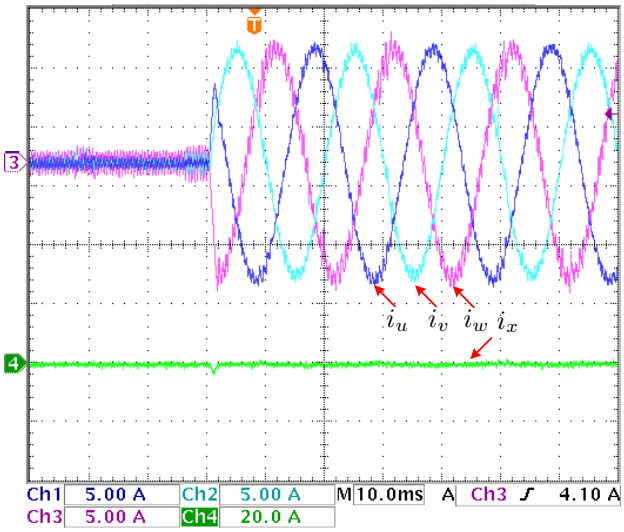

Figure 11. Results for Case-7 – unbalanced loads with step change in balanced reference currents.

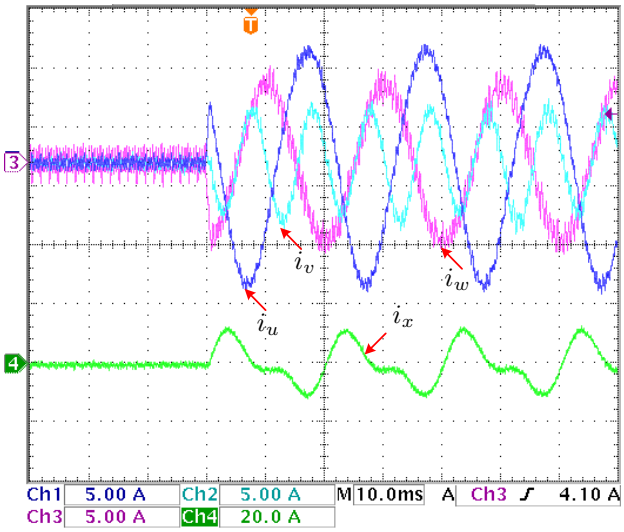

Figure 12. Results for Case-8 – unbalanced loads with step change in unbalanced reference currents.

results in steady-state, with unbalanced loads and unbalanced references, are presented in Fig. 10. Similar to Case-2, the neutral current, which is not sinusoidal in nature, flows through the neutral leg. The magnitude of load and neutral currents are observed to be the same as Case-2, and thus it is evident that the load and filter parameter variations do not affect the reference tracking. This is one of the prominent features of the proposed digital controller. The FFT window for current i_u of this case is comparable to Case-2.

For this case, the THD for currents i_u, i_v and i_w, are 6.89%, 12.66% and 21.38%, respectively. The results for Cases 7 and 8 with step-change in loads from 0A to Case-5 and Case-6 are presented in Figs. 11 and 12. Similar to Cases-3 and 4, fast dynamic response with no overshoot for load currents is observed in both cases.

V. Conclusion

In this paper, a digital predictive control technique for the current control of four-leg inverters is presented. In contrast to the previously proposed control schemes, this method is simple and intuitive for real-time implementation. With this method, complex issues such as design of internal current control loops, tuning of PI controllers, small-signal modeling of inverter for stability analysis, and development of a modulation stage can be avoided with no negative effect on the steady-state and transient-state operation. The predictive algorithm uses the discrete nature of power converters to predict the future load currents for all 16 switching states. Then, with the help of the cost funcion, the algorithm compares the different predictions to the projected reference currents. The ideal minimum of the cost function is zero, and it represents perfect regulation of the load currents to their references. The proposed control scheme can compensate perturbations in load and filter parameter changes without significantly affecting the transient and steady-state response.

Further research on predictive control with impedance variations, parameter adjustments, high frequency noises, and comparison to the classical control schemes is considered for future works.

Appendix

The parameters used in the simulation and experimental tests are summarized in Table I.

Table I
Two-level four-leg inverter and load nominal parameters

Variable	Description	Value
v_{dc}	DC-link voltage	150V
$R_{fu,v,w,x}$	Filter resistance	0.05Ω
$L_{fu,v,w,x}$	Filter inductance	6mH or 12mH
$R_{u,v,w,x}$	Load resistance	2.5Ω *or* 5Ω
$f^*_{u,v,w}$	Reference nominal frequency	50Hz
$I^*_{u,v,w}$	Reference nominal peak current	10A
T_s	Sampling time	66.67μs

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