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Article

Simulation Model to Analyze the Consequences of DC Faults in MMC-Based HVDC Stations

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Abstract: The global development of high-voltage direct-current (HVDC) systems in fields such as renewable energy sources, interconnection of asynchronous grids or power transmission over great distances, is unquestionably important. Though widely used, the modular multilevel converter with half-bridge cells is sensitive to DC pole-to-pole faults and the time-response of the protections is critical. Reliability and availability are paramount: circuit-breakers must minimize the effects of any fault on the converter, while ensuring rapid restart. This paper focuses on the modelling aspects to analyse the behaviour of HVDC stations during DC pole-to-pole faults, using either AC or DC circuit-breakers, with different parameters. The proposed model can represent the main issues met by the converter cells during DC faults, such as semiconductor overcurrents and overvoltages, allowing a proper design of the cells.

Keywords: modular multilevel converter (MMC); simulation; high-voltage direct-current (HVDC); DC fault



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1. Introduction

High-voltage direct-current (HVDC) has had significant development over the last fifty years. After mercury-arc valves, the introduction of the thyristor in 1972 for the Eel River project confirmed the potential of solid-state valves [1]. Today, powers exceeding 5 GW are transmitted through line-commutated converters (LCCs), over distances greater than 2000 km [2]. Over the last ten years, the Modular Multilevel Converter (MMC), based on Voltage-Source Converter (VSC) technology, has become popular for such applications leading to lower costs, lower footprint and “black-start” capability. These features are particularly relevant for renewable energy applications: in Germany for instance, grid-connection of remote offshore windfarms is based on this topology.

LCCs have relatively high line-impedance as they belong to the family of Current-Source Converters (CSCs), so in the event of a DC fault, the rise of the current is slow enough to allow protection with AC circuit-breakers [3], which typically operate within 70 ms [4,5]. This current limitation is missing with the MMC using half-bridge cells [6], so DC fault becomes a critical issue. The modular multilevel converter does not have a central DC bus capacitor but the arm inductors do contribute to fault current limitation [7]. When a DC fault occurs, the converter turns into an uncontrolled diode-rectifier, requiring the components to withstand high voltage and current stresses, and the purpose of this paper is to investigate modeling methods to properly size the converter and to select the most suitable protection. Based on PLECS, the model aims to predict the potential issues during DC pole-to-pole faults, by considering the dynamics of the different subsystems.

2. Case of Study

2.1. Presentation of the System

A symmetric monopole HVDC link has been selected, shown in Figure 1, a configuration typically used for offshore wind-parks. The total DC link voltage is twice that of the pole-to-ground voltage, which allows a reduction of the DC link current for a lower voltage rating of the cables. CIGRE, the Council on Large Electric Systems, works on high-voltage equipment and offshore systems. Through working groups, generally composed of people from various transmission system operators (TSOs), it develops recommendations for the testing and design of such systems and has also developed a generic DC grid-test system [8]. Each grid is connected to a converter through a delta-wye transformer or wye-delta transformer, the DC transmission distance is equal to 200 km. Since a symmetric monopole configuration has no natural connection to the ground, a star-point reactor must be used [9,10].

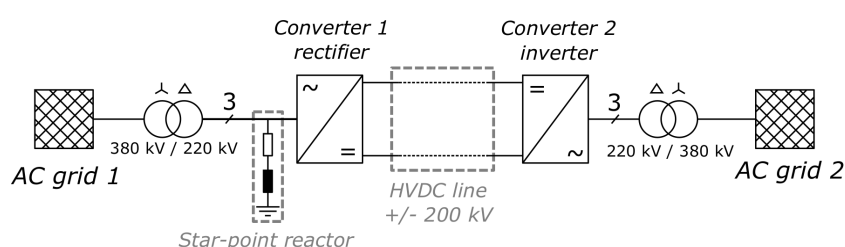


Figure 1. Overview of the symmetric monopole high-voltage direct-current (HVDC) link; Converter 1 operates as a rectifier and Converter 2 operates as an inverter.

The modular multilevel converter (MMC) is presented in Figure 2a. A cluster is composed of N cells, as illustrated in Figure 2b. A cluster behaves like a controlled voltage source, while arm-inductors allow the regulation of arm-currents. Switches T_1 , T_2 , D_1 and D_2 are generic and “ideal”: they behave like two-quadrant devices, where the anti-parallel association of T_1 and D_1 (or T_2 and D_2) allows the current to flow in either direction, depending of T_1 's state (or T_2 's state). Ideal waveforms are represented in Figure 3 and show that arm-currents contain both a DC component and a grid-frequency component. Between the upper and lower arms, the AC component is shifted by 180° . To get bidirectional power flow, cells must provide either current reversibility or voltage reversibility and in fact, current reversibility is chosen to obtain smaller RMS currents and easier reactive power injection [11]. Half-bridge cells with generic turn-off devices are used, as shown in Figure 2b.

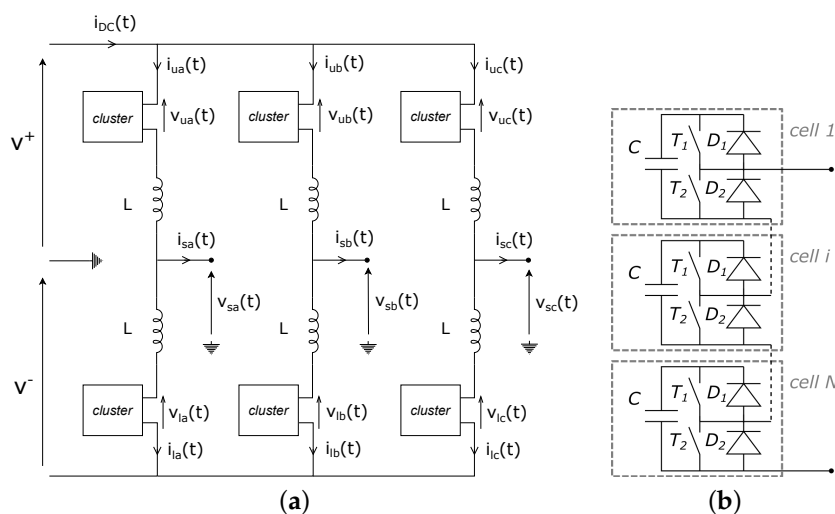


Figure 2. Overview of the modular multilevel converter. (a) Modular multilevel converter. (b) Cluster with half-bridge cells.

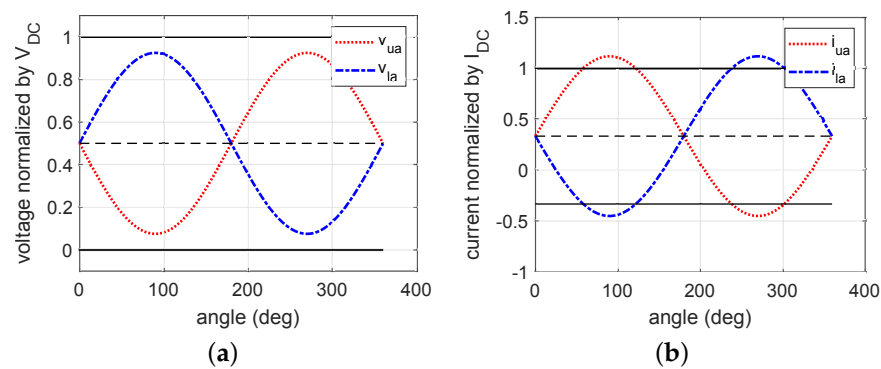


Figure 3. Arm-voltages and arm-currents of MMC with half-bridge cells. (a) Voltages. (b) Currents.

The modular multilevel converter benefits from low di/dt since arm-currents are sinusoidal, low dv/dt because of the large number of levels, and a high degree of modularity. This feature is becoming more and more appreciated in power electronics as it reduces costs and ensures easier maintenances. The MMC structure is also suitable for a large range of powers. In the field of HVDC, the number of cells N is typically a few hundred: total harmonic distortion is so low that filters are no longer required [12]. The main characteristics of the converter are summarized in Table 1. An active power of 800 MW is typical, according to recent HVDC-MMC projects [2]. The equivalent cell resistance R_{cell} represents the power losses of one cell, mainly due to the conduction losses of the semiconductors. Total resistance per arm is NR_{cell} .

Table 1. Electrical characteristics of the HVDC link.

Name	Symbol	Value
Active power	P	800 MW
DC bus voltage	$V_{DC,nom}$	± 200 kV
Arm inductor	L	29 mH
Cell capacitance	C	10 mF
Number of cells	N	200
Equivalent cell resistance	R_{cell}	1.361 m Ω

2.2. Definition of the Fault

A DC pole-to-pole fault is defined as a short-circuit between positive and negative converter poles. In the steady-state, if nothing is done to interrupt the power flow, fault currents may reach between five and ten times the nominal values [8]. Such situations can lead to the destruction of many converter components, which would require lengthy shutdowns. Thus, this kind of fault is critical and must be properly handled. Here a DC pole-to-pole fault is represented by a series association of a resistor and an inductor; which is necessary to get consistent waveforms from the simulation software.

2.3. Protection Strategy

The response of the MMC to a DC pole-to-pole fault depends on the topology of the cells. Inherent DC fault ride-through capability is obtained when the converter is able to prevent the transfer of power from the AC to the DC side. It requires a decoupling between the AC grid-voltages and the DC link voltage, which is not the case with half-bridge cells [13]. Only full-bridge cells and hybrid structures, using different types of cells in the same cluster, may provide DC fault ride-through capability. This feature, though appreciable for HVDC applications, carries an important cost as it leads to an increase in the number of devices, hence higher cost and lower efficiency [14,15]. Consequently MMCs based on half-bridge cells must rely on additional protections against DC pole-to-pole faults.

2.3.1. Behaviour of the System during Faulty Operation

Many steps should be distinguished when a fault occurs [16,17]:

1. Fault propagation, it firstly affects the closest elements;
2. Fault detection, a logical controller decides from a list of conditions whether a DC fault has occurred or not;
3. Blocking of the controlled devices; Insulated-Gate Bipolar Transistors (IGBTs) de-saturate if their on-state currents exceed their ratings which quickly leads to their destruction if not turned off in time [18]. In the case of Integrated Gate-Commutated Thyristors (IGCTs), the issues are similar: they might be switched off beyond of their safe operating areas since the arm-currents rise quickly. After blocking the controlled devices, the converter behaves like a diode-rectifier [10,13].
4. Breaking-time, it starts as soon as a fault is detected. This time depends on the breaking technology used.
5. Fault clearance, faulty systems are isolated from the rest of the grid and residual energy is dissipated. The corresponding duration strongly depends on the grid configuration, which includes cables and AC transformers.

2.3.2. Fault Detection

Two issues are particularly crucial for fault detection [19,20]:

- Speed, because slowness is a vicious circle: the slower the protections, the higher the current and voltage stresses; this means that fast protections result in smaller fault currents allowing, for instance, lower ratings;
- Reliability, fault-detection must not produce “false positives” during normal operation or when disturbances occur, yet still not missing any real faults for which is the protection was designed.

To achieve a satisfactory compromise between speed and reliability, the following principal are implemented:

1. Undervoltage protection on the DC link [20,21], too large a voltage-drop is deemed due to a short-circuit. Even if the method is often mentioned in the literature, numeric values are not systematically proposed. 50% of the nominal DC link voltage $V_{DC,nom}$ is considered as a relevant and restrictive threshold [22];
2. Overcurrent protection in the arms [23], as mentioned, the controlled devices are turned off to avoid their destruction if the arm-currents are too high. In the case of Integrated Gate-Commutated Thyristors (IGCTs), the maximum current is set to 75% of the maximum controllable turn-off current since this value must not be exceeded [24]. With Insulated-Gate Bipolar Transistors a higher value would have been chosen, typically 90% of the peak forward current [25];
3. Overcurrent protection for the DC link [20,26], a threshold value of 150% of the maximum nominal DC link current is assumed [27].

Faster and more robust methods exist, for instance, based on traveling wave theory or communication systems between the converters [20,21,28]. Communication systems could theoretically be very efficient since fault-detection can be transmitted to the other converters of the HVDC link before the fault propagates itself. A delay of 100 μ s is applied to all software protections between the controls and the power semiconductors, to allow for internal sources of delay in the system.

3. Models for HVDC Link with MMCs during Normal Operation

3.1. Converter

According to Table 1, the converter contains almost 5000 discrete devices. A simulation model implementing all the devices would have an important computation time, the number of steps being higher because the state-space system is larger. Many references [11,29] have thrown light on the value of using an averaged model, to eliminate this drawback. The principle lies in a large number of cells in an HVDC-MMC since the influence of

switching is not visible in the waveforms; the applicable hypotheses are summarized in Table 2.

Table 2. Assumptions considered to model a modular multilevel converter (MMC) cluster.

Model with Discrete Devices	Averaged Model
Perfect power switches	Low harmonic distortion
Perfect cell capacitor	Large number of cells

Power switches are considered “ideal” in that their change of state is instantaneous, with no losses. The cell capacitor is assumed perfect, its model could be more complex for specific needs (self-discharge or aging for instance). The transition from this model to the averaged model requires low harmonic distortion due to the modulation method: this condition is utterly fulfilled since beyond a certain number of cells per cluster, filter requirements are eliminated [29]. Therefore, the series association of cells can be replaced by a single cell to obtain an averaged model of the cluster, containing:

- An equivalent capacitor;
- A voltage source, controlled by the instantaneous duty-cycle;
- A current source, controlled by the instantaneous duty-cycle.

This simplification is illustrated in Figure 4b. α is the instantaneous duty-cycle, provided by the inner control loops. It must be noted that output waveforms no longer depend on the modulation strategy nor the cell balancing method; their influence is neglected, as detailed in Table 3. On the other hand, converter dynamics remain accurately modeled, as inner control loops and voltage and power controls are still implemented. Figure 4c is exactly the same model as presented in Figure 4b but the voltage source and the current source have been separated and this representation is kept.

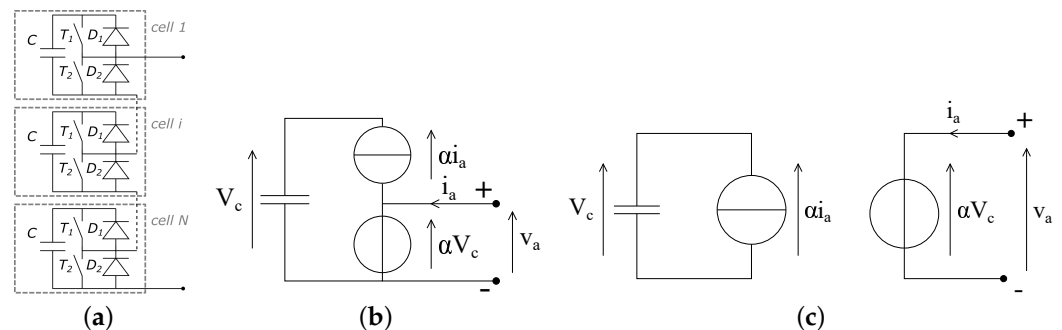


Figure 4. Models for simulation of MMC in normal operation. (a) Real cluster. (b) Averaged model of the cluster. (c) Averaged model of the cluster divided into two parts.

Table 3. Comparison between the model with discrete devices and the averaged model.

Modelling of...	Model with Discrete Devices—Figure 4a	Averaged Model Figure 4b,c
...semiconductor	-	-
switching transients	no	no
...modulation strategy	yes	no
...cell balancing	yes	no
...semiconductor losses	yes	no
...inner control loops	yes	yes
...voltage and power control	yes	yes

3.2. Control

To facilitate the implementation of the control strategy, the following transformation is applied to arm-voltages and arm-currents:

$$\begin{aligned} v_{sum,i}(t) &= \frac{v_{ui}(t)+v_{li}(t)}{2}, i \in \{a,b,c\} \\ v_{diff,i}(t) &= \frac{-v_{ui}(t)+v_{li}(t)}{2}, i \in \{a,b,c\} \\ i_{sum,i}(t) &= \frac{i_{ui}(t)+i_{li}(t)}{2}, i \in \{a,b,c\} \\ i_{diff,i}(t) &= \frac{i_{ui}(t)-i_{li}(t)}{2}, i \in \{a,b,c\} \end{aligned} \quad (1)$$

Equation (1) allows a simplification of the MMC equations, leading to the equivalent circuit of Figure 5 for “diff” components, where $i \in \{a;b;c\}$ designates the phase. It is worth mentioning that voltage drop due to arm-inductors and semiconductors is negligible compared to arm inductor voltages and grid voltages.

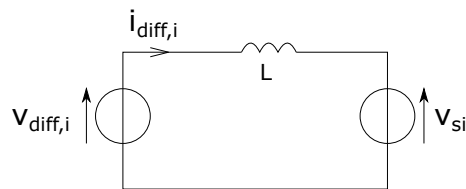


Figure 5. Equivalent circuit for “diff” components, $i \in \{a;b;c\}$.

A dq0 transformation is relevant for the control of a three-phase MMC, since arm-voltages and arm-currents contain both zero-sequence and positive-sequence components. For Figure 5, the following equations are obtained:

$$\begin{cases} L \frac{di_{diff,d}}{dt}(t) = L\omega_0 i_{diff,q}(t) + v_{diff,d}(t) - v_{sd}(t) \\ L \frac{di_{diff,q}}{dt}(t) = -L\omega_0 i_{diff,d}(t) + v_{diff,q}(t) - v_{sq}(t) \end{cases} \quad (2)$$

$v_{sd}(t)$ and $v_{sq}(t)$ are the (d,q) components of the grid voltages ($v_{sa}(t), v_{sb}(t), v_{sc}(t)$) as defined in Figure 2a. The equivalent circuits of Equation (2) are shown in Figure 6. In can be observed that the transformation lead to coupled relations between the d and q axes.

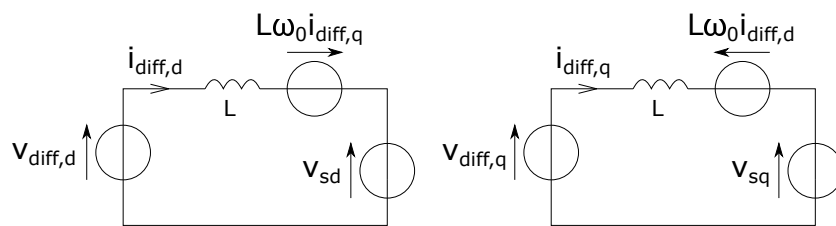


Figure 6. Equivalent circuits of the converter in the dq plane, for output-current control.

Thus, the resulting output-current controller, shown in Figure 7, includes decoupling terms to compensate for the existing couplings.

For the PI controller, a bandwidth of $2\pi \cdot 30$ rad/s is high enough to ensure a satisfactory dynamic response. An anti-windup protection is implemented, if the voltage $v_{ns,d}(t)$ (or $v_{ns,q}(t)$) reaches a given limit, the reference output voltage $v_{diff,d}^*(t)$ (or $v_{diff,q}^*(t)$) saturates. Then the difference between the limit and $v_{ns,d}(t)$ (or $v_{ns,q}(t)$) is used to limit the integration. Duty-cycles are calculated by dividing the reference voltages $v_{u,abc}^*(t)$ and $v_{l,abc}^*(t)$ by the nominal DC link voltage, V_{DC} , using the following formula:

$$\underline{\alpha}_{u,abc}(t) = \frac{v_{u,abc}^*(t)}{V_{DC}} \quad \text{and} \quad \underline{\alpha}_{l,abc}(t) = \frac{v_{l,abc}^*(t)}{V_{DC}} \quad (3)$$

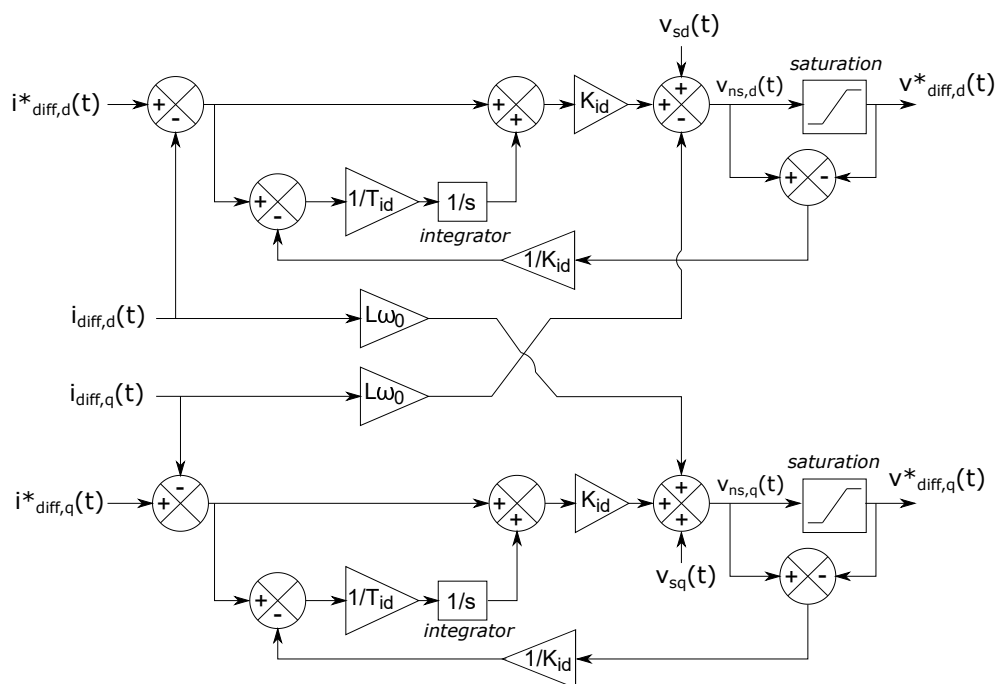


Figure 7. Block diagram of the output-current controller.

“Direct voltage control” (DVC), this strategy provides asymptotic stability of the arm-energies [30,31] while however introducing circulating currents in the converter, because the total capacitor voltage has a ripple at both grid-frequency f_0 and twice grid-frequency. Thus, a circulating current suppression controller (CCSC) is implemented [32], as shown in Figure 8. As the second-order harmonic is the most significant, only this harmonic is suppressed. The first unwanted harmonic appears at four times the grid frequency, but its influence is barely visible from a distortion point of view. The approach proposed by Figure 8 points out that output-current controller and CCSC are decoupled, since the output-current controller operates along the “diff” components, in the dq0 plane, whereas CCSC delivers “sum” components in the dq0 plane. Afterwards, reverse transformations are performed to recover “diff” and “sum” components in the abc plane and finally the six arm-voltages $v_{u,abc}(t)$ and $v_{l,abc}(t)$.

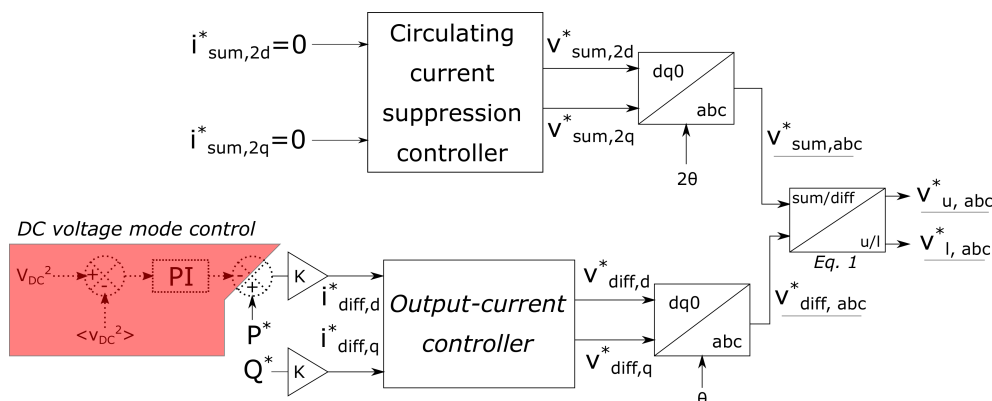


Figure 8. Simplified block diagram of the overall control system.

As illustrated in Figure 1, the two converters are connected through a DC link. In such a connection, the overall control strategy is for one converter to control the transfer of power while the other manages the DC bus voltage [9], using the “DC voltage mode control”.

4. Models for the HVDC Link with MMCs during Faulty Operation

4.1. HVDC Cables

4.1.1. Modelling with pi-Sections

Pi-sections [33] are a basic way to model DC cables. The relation between the number of pi-sections and the modeling error of the line has been shown to depend on the line's resonant frequency [34]. It presents the limits bound to pi-sections which are dedicated to modeling low-frequency phenomena. These limitations have been confirmed and a more accurate model, the FD- π model, has been proposed [33]. A comparison with the real impedance of an HVDC cross-linked polyethylene extruded (XLPE) cable shows that resonances are damped, while the representation with pi-sections results in sharp variations at the resonant frequencies. Simulations using pi sections are characterized by high-frequency ripples which are not realistic, because of the discrete resonant frequencies of the model.

4.1.2. Modelling with Travelling Wave Theory

Traveling wave theory lies in local equations instead of discrete passive components. This more accurate representation is chosen in PLECS to avoid the drawbacks of pi sections. The corresponding implementation in PLECS simulation software is based on [35].

The characteristics of the ± 200 kV cable are shown in Table 4.

Table 4. Macroscopic characteristics of a ± 200 kV DC cable [8].

Name	Symbol	Value
Resistance per km	r_{cable}	11 m Ω /km
Inductance per km	l_{cable}	2.615 mH/km
Pole-to-ground capacitance per km	c_{cable}	0.2185 μ F/km
Conductance per km	g_{cable}	0.055 μ S/km

4.2. Converter

After the blocking of the controlled devices, the MMC has the configuration shown in Figure 9. It shows that the capacitors cannot be discharged, which is an appreciable feature of the MMC: there is no discharge of energy in the DC link due to the passive components of the converter. On the other hand, capacitors can be charged during short durations and this may lead to significant overvoltages because of the large currents during faults.

The previous averaged model, suitable for normal operation, is no longer valid after the blocking of the controlled devices. Based on Figure 9, the model after fault detection is represented in Figure 10a. If the arm-current is positive, only the upper diodes of the cells conduct and all the cell capacitors are charged whereas if the arm-current is negative, only the lower diodes conduct and the upper diodes are blocked. Some similarities are observed between this model and the averaged model of the cluster during normal operation and it is then possible to combine them to obtain a single model, suitable whatever the mode of operation is. The final model is presented in Figure 10b. CE is equal to 1 during normal operation, i.e., the switch is closed to obtain the circuit of Figure 4c. When the controlled devices are opened CE is equal to 0, i.e., the switch is opened. Furthermore, the expressions of the capacitor current i_c and voltage v' depend on the mode of operation:

$$\begin{cases} \text{if } CE = 1 \text{ (switch closed), } v' = \alpha V_c \text{ and } i_c = \alpha i' \\ \text{if } CE = 0 \text{ (switch opened), } v' = V_c \text{ and } i_c = i' \end{cases} \quad (4)$$

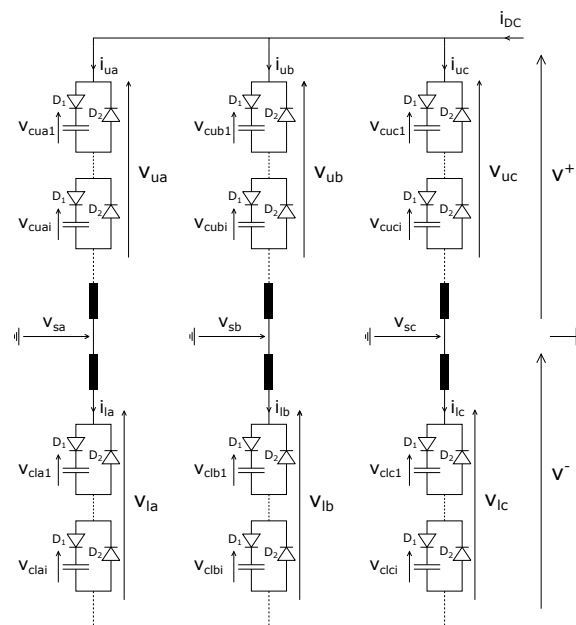


Figure 9. MMC with half-bridge cells after blocking of the controlled devices.

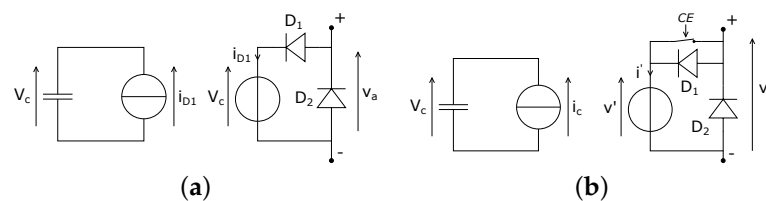


Figure 10. Averaged models for MMC simulation under faulty operation. (a) Averaged model of the cluster during faulty operation; all controlled devices are blocked. (b) Averaged model for normal and faulty operation; the switch is closed during normal operation and opened during faulty operation.

4.3. High-Voltage Circuit Breakers (CBs)

4.3.1. Considerations for DC Circuit-Breakers

Direct-current has no zero-crossing, so a DC circuit-breaker must withstand high overvoltages when breaking the full fault-current [5] and it must open quickly to limit the prospective fault current [36] as well as generating negligible losses when closed. Different families of DC circuit-breakers exist; hybrid and active current injection circuit-breakers exhibit excellent performances with opening times lower than 10 ms and breaking current capabilities of about 15 kA [37]. The DC circuit-breaker presented in Figure 11 is selected, it contains a main current path, a commutation path and an energy absorption path (metal-oxide varistors) which dissipates a significant amount of the system’s magnetic energy and limits the transient interruption voltage (TIV). A fault-current limiter is added to limit the maximum current derivative (di/dt) prior to breaking and ensures that the DC circuit-breaker remains within its rated current capability. For this study, a maximum rate of rise of 6 kA/ms is assumed [26] for the DC link current. From this criterion, the arm inductors of the closest converter should be considered. The circulating component of arm-currents sees an inductance of $2L$, so the total inductance seen from the DC link is $\frac{2}{3}L$. Thus, the fault-current limiter should have the following value:

$$2 \cdot L_{FCL} = \frac{V_{DC}}{\left(\frac{di_{DC}}{dt}\right)_{MAX}} - \frac{2}{3}L \approx 45 \text{ mH}, \text{ with } \begin{cases} V_{DC} = \pm 200 \text{ kV} \\ \left(\frac{di_{DC}}{dt}\right)_{MAX} = 6 \text{ kA/ms} \\ L = 29 \text{ mH} \end{cases} \quad (5)$$

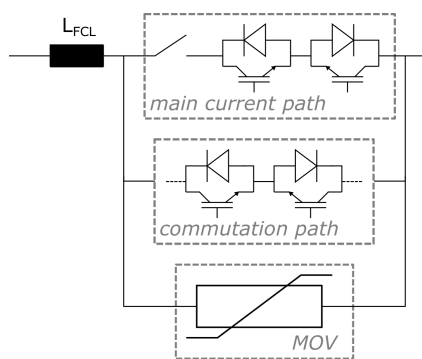


Figure 11. Generic hybrid DC circuit-breaker selection.

Such a value appears reasonable according to the literature, which provides a wide choice of fault-current limiters with various criteria [26,38,39].

During normal operation, the current flows through the main current path. This main current path is generally composed of a low-loss mechanical switch and a power electronic switch. When a fault is detected, the power-electronic switch opens, which diverts the current to the commutation path; then the mechanical switch opens to protect the power-electronic switch against the subsequent transient interruption voltage. The opening of the commutation path generates the transient interruption voltage, which triggers the conduction of the metal-oxide varistors. The diversion of the current from the main path to the commutation path and the opening of the commutation path are modeled by a pure delay, since it is the internal operation of the circuit-breaker. A delay of 3 ms [19] is deemed reasonable to represent the breaking-time of the DC circuit-breaker. The metal-oxide varistors (MOV) can be modeled by a series association of constant voltage sources and a non-linear resistor thus obtaining a logarithmic approximation of the MOV’s v-i characteristics. In this study, they are defined by a nominal discharge current of 12 kA at a lightning impulse protection level of 600 kV.

Table 5 summarizes the numeric values retained for the passive elements. According to Figure 12, four DC circuit-breakers are used but to avoid interferences in the waveforms, the tripping of the DC circuit-breakers in the positive poles of the two converters is delayed by 7 ms for the simulation.

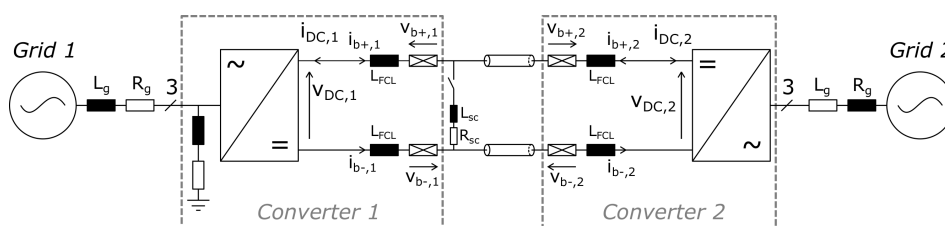


Figure 12. Detailed model of the HVDC link with DC circuit-breakers and notations.

Table 5. Numeric data for the passive elements of the HVDC link.

Name	Symbol	Value
Transformer leakage inductance	L_g	35 mH
Transformer series resistance	R_g	0.363 Ω
Grid phase-to-phase voltage	U_g	220 kV
Short-circuit resistance	R_{sc}	1 m Ω
Short-circuit inductance	L_{sc}	100 nH
Fault-current limiter	L_{FCL}	22.5 mH

4.3.2. AC Circuit-Breakers

The AC circuit-breaker is modeled in a simpler way: its response time is very long compared to its turn-off dynamics. Furthermore, it opens when the current crosses zero. Thus, a TRIAC controlled by a delayed signal is an accurate representation. A delay of three grid periods, i.e., 60 ms at $f_0 = 50$ Hz, is assumed.

5. Results

The system starts at the nominal DC link voltage $V_{DC,nom}$ of 400 kV. Active power is set to 800 MW, no reactive power is injected. At $t_0 = 4$ s, when a steady-state operation is reached, the positive and negative poles of Converter 1 operating as a rectifier are short-circuited, as shown in Figure 12. It should be noted that this is a critical case of study for Converter 1: DC link current already flows in the direction of the short-circuit, which increases the maximum fault current.

5.1. Fault Detection

Table 6 summarizes the protections that triggers after a DC pole-to-pole fault with AC circuit-breakers. It appears that undervoltage detection is very efficient, since the short-circuit is made at the point where the DC link voltage is measured. It leads to a total detection duration of 100 μ s. This duration, though optimistic, does not significantly affect the overall behavior of the HVDC link: the opening time of the AC circuit-breakers being much greater than the detection duration. Converter 2 detects the fault later, after $\Delta t = 3.48$ ms. It corresponds to the time for the short-circuit to spread over the DC cables, knowing that Converter 2 is separated from Converter 1 by a distance of 200 km.

Table 6. Protection method that triggers for each converter with AC circuit-breakers

Converter	Nature of the Protection	Duration	Total Duration with Internal Delays
1 (rectifier)	undervoltage	0 s	100 μ s
2 (inverter)	undervoltage	3.38 ms	3.48 ms

Table 7 provides the same information for the DC circuit-breakers. Converter 1 detects an overcurrent in the DC link before an undervoltage. However, Converter 2 detects an undervoltage at the same time as in the case of AC circuit-breakers.

Table 7. Protection method that triggers for each converter with DC circuit-breakers

Converter	Nature of the Protection	Duration	Total Duration with Internal Delays
1 (rectifier)	overcurrent (DC link)	172 μ s	272 μ s
2 (inverter)	undervoltage	3.38 ms	3.48 ms

5.2. Comparison between AC Circuit-Breakers and DC Circuit-Breakers

5.2.1. Waveforms

Figure 13a shows that the fast opening-time of the DC circuit-breakers significantly reduces the constraints on the system: the peak DC link current is less than 10 kA with DC circuit-breakers, while it is greater than 20 kA with AC circuit-breakers. Besides, the duration of fault-limitation is much greater with AC circuit-breakers; Figure 13b shows that approximately 70 ms are required to open the three AC circuit-breakers of Converter 1. Even after the opening of the AC circuit-breakers, the fault is still not cleared because the short-circuit has created an inductive closed loop which allows the circulation of arm-

currents. It explains why a non-zero DC link current remains even after the opening of the AC circuit-breakers in Figure 13a. The time-constant of this phenomenon is:

$$\tau = \frac{L}{NR_{cell}} = 106 \text{ ms, with } \begin{cases} N = 200 \\ R_{cell} = 1.36 \text{ m}\Omega \\ L = 29 \text{ mH} \end{cases} \quad (6)$$

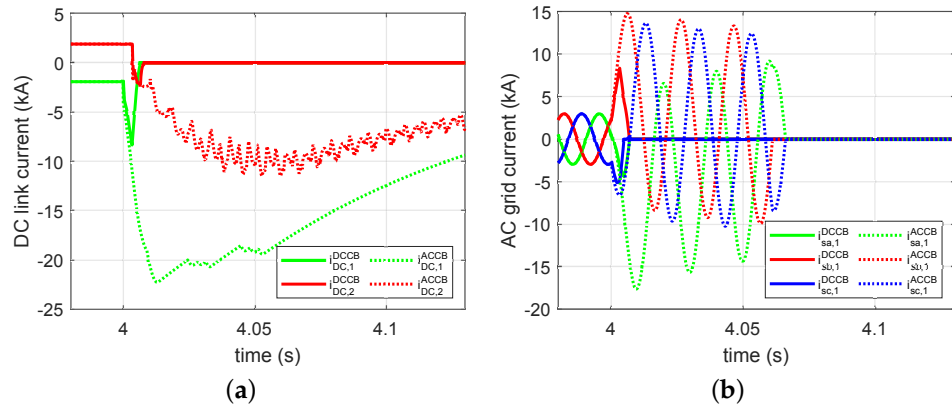


Figure 13. DC link current and AC grid currents during DC pole-to-pole fault with AC circuit-breakers (dotted lines) and DC circuit-breakers (solid lines). (a) DC link current - zoom - green for Converter 1, red for Converter 2, solid line for DC CBs and dotted line for AC CBs. (b) AC grid currents $i_{s,i}(t), i \in \{a; b; c\}$, green for phase a, red for phase b and blue for phase c, solid line for DC CBs and dotted line for AC CBs.

This phase is critical because of its duration, which is another drawback of AC circuit-breakers: contrary to a converter fitted with DC circuit-breakers, fault-clearance takes several hundred milliseconds. The arm-currents slowly decrease as seen in Figure 14 and the energy is dissipated through the inductors' resistances and the diodes. Figure 13a also shows that the position of the short-circuit greatly affects fault currents: the DC link current of the rectifier (Converter 1) quickly rises, while the DC link current of the inverter (Converter 2) has a smaller rate-of-rise. This is due to the impedance of the DC cable, which attenuates and delays the effects of the short-circuit since Converter 2 is at $D = 200$ km of the short-circuit.

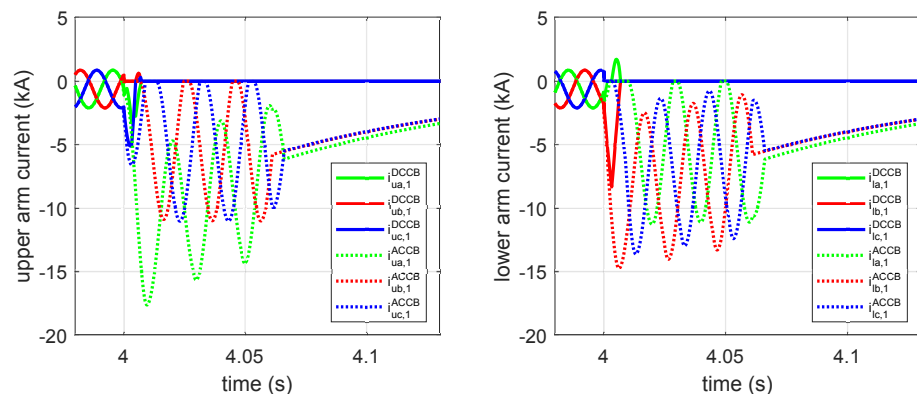


Figure 14. Upper and lower arm-currents during DC pole-to-pole fault with AC circuit-breakers (dotted lines) and DC circuit-breakers (solid lines); green for phase a, red for phase b and blue for phase c.

5.2.2. Surge Current Integrals

From Figure 14 it is possible to calculate the surge current integrals of the diodes in each cluster, according to the following formula:

$$I^2t = \int_{t=4s}^{+\infty} (i_{Diode}(t))^2 dt \quad (7)$$

As explained in Section 2.3.1, the converter tends to behave like a diode-rectifier after a DC pole-to-pole fault. As shown in Figure 9, while diodes D_1 are blocked, diodes D_2 are involved in the fault, thus making surge-current capability an important issue for these diodes.

Table 8 shows the surge current integrals for diodes D_2 in the different arms of Converter 1 with AC circuit-breakers; the maximum is $8.60 \text{ MA}^2\cdot\text{s}$. This value can be compared to some high-power diodes proposed by different manufacturers, presented in Table 9. It appears that individual press-pack diodes have higher surge current integrals; hybrid IGBT or IEGT packages do not withstand the required surge current integrals. It explains some technological choices made by manufacturers:

- Siemens uses a press-pack thyristor to bypass the diodes D_2 during faulty operation [40];
- RXPE considers the use of press-pack diodes to withstand the surge current integral [41];
- ABB has similar considerations, cells based on IGCT have a full short-circuit failure mode (SCFM) which allows the removal of the bypass switch to use a single bypass thyristor to discharge the cell capacitor [42,43].

Table 8. Surge current integral ($\text{MA}^2\cdot\text{s}$) for D_2 in Converter 1 with AC circuit-breakers.

Phase	a	b	c
upper arms	8.60	4.36	4.15
lower arms	4.88	6.47	5.42

Table 9. Surge current integral ($\text{MA}^2\cdot\text{s}$) for typical 4.5 kV devices.

Manufacturer	Device	Technology	I^2t ($\text{MA}^2 \cdot \text{s}$)
ABB	5SNA 2000K450300	press-pack IGBT + diode	5.12
ABB	5SDF 20L4520	single press-pack diode	10.1
Infineon	D1961SH45T	single press-pack diode	8.0
Infineon	D4600U45X172	single press-pack diode	32.0
Toshiba	ST1500GXH24	press-pack IEGT + diode	0.5

The conclusion is different with DC circuit-breakers, as shown in Table 10, surge current integrals are much smaller because of the drastic reduction of fault-interruption time. Among the list of devices of Table 9, all are compatible with the case study. Therefore the investment in a DC circuit-breaker is mitigated by the removal of a bypass thyristor. It also allows the use of devices with integrated diodes, with smaller surge-current integrals, for instance, 5SNA 2000K450300 of ABB or ST1500GXH24 of Toshiba according to Table 9.

Table 10. Surge current integral ($\text{MA}^2\cdot\text{s}$) for D_2 in rectifier with DC circuit-breakers.

Phase	a	b	c
upper arms	0.026	<0.001	0.075
lower arms	<0.001	0.18	<0.001

5.3. Behaviour of the DC Circuit-Breaker (DCCB)

Figure 15 shows voltages and currents of the two first DC circuit-breakers to open: the first one is located in the negative pole of Converter 1, the second is located in the negative pole of Converter 2. In the beginning, the DC link current of Converter 1 rises quickly, at a rate mostly determined by the fault-current limiters L_{FCL} . The first DC circuit-breaker limits the fault after $\Delta t = 3.27 \text{ ms}$ and breaks a current of 8.34 kA. This time is the sum of the detection delay, 271 μs and the internal current commutation time of the

DC circuit-breakers, assumed equal to 3 ms. It induces the transient interruption voltage, defined by the v - i characteristics of the MOV and rises to slightly less than 600 kV, i.e., 150% of the DC link voltage $V_{DC,nom}$. From this moment on, the DC link current decreases in absolute value and reaches zero within 3.2 ms, which corresponds to an average current slope of 2.6 kA/ms. Due to the duration of detection and the internal current commutation-time of the DC circuit-breaker, the second DC circuit-breaker neutralizes the fault after $\Delta t = 6.48$ ms. It occurs after the inversion of the DC link current' sign, induced by the short-circuit in the other extremity of the DC line. The associated TIV is smaller and fault current suppression time is shorter, because the circuit-breaker opens at 2.21 kA, which is much lower than that of the first DC circuit-breaker. Therefore, the fast operation of the DC circuit-breaker in Converter 1 has reduced the fault currents seen by Converter 2.

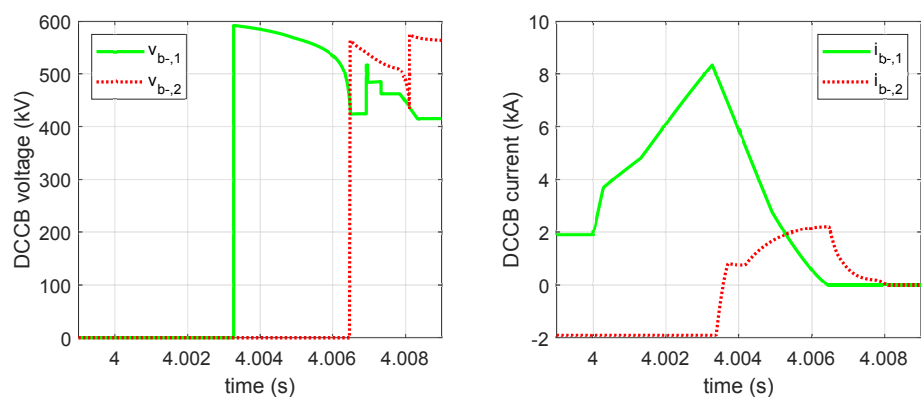


Figure 15. Voltage and current of the lower DC circuit-breakers during DC pole-to-pole fault.

5.4. Overvoltages during Faulty Operation

Figure 16 shows the capacitor voltages of Converter 1 during DC pole-to-pole fault with DC circuit-breakers. These capacitors represent those of the averaged model of a cluster: they represent the sum of the capacitor-voltages of all the cells, for a given cluster. Some of these capacitors are charged during the fault current suppression time of the DC circuit-breakers; this phenomenon is due to:

- The insertion of a large voltage between the ground and the negative pole by the DC circuit-breaker. This voltage exceeds the nominal DC link voltage and is not shared between the two poles. The lower arm-voltage is too low, while the grid voltage of phase a is the highest. Consequently, a positive arm-current must flow in the lower arm of phase a. This current is visible in the right part of Figure 14 in green.
- The diminution of the voltage between the positive pole and ground, the upper arm-voltages are too low then diodes D_1 cannot be reverse-biased, which induces positive arm-currents.

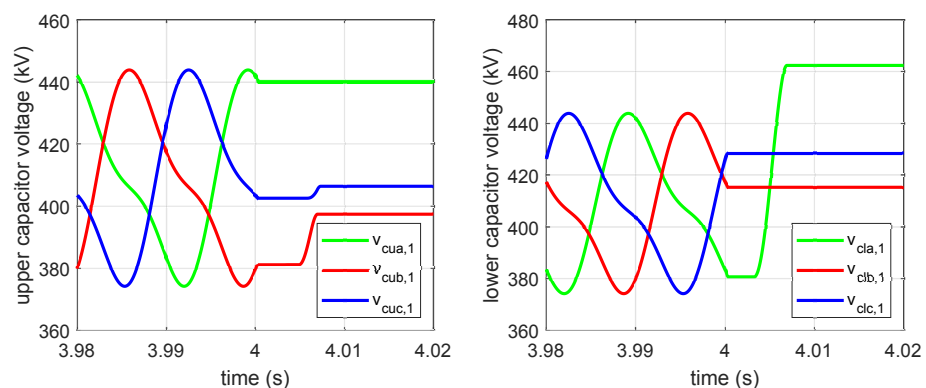


Figure 16. Capacitors voltages during DC pole-to-pole fault with DC circuit-breakers $v_{cu,i}(t)/v_{cl,i}(t), i \in \{a; b; c\}$, green for phase a, red for phase b and blue for phase c.

This phenomenon stops at the end of the fault current suppression time, since the circulation of arm-currents is no longer possible. For this case study, the maximum capacitor voltage reaches 116% of its nominal value. The over-charging of the arm capacitors is dangerous as it can damage the capacitors as well as the semiconductors. On the other hand, the maximum capacitor voltages depend on the MOVs characteristics and other parameters: AC line impedance and characteristics fault-current limiters, for instance. Grounding of the system, realized with a star-point reactor for symmetric monopole configurations, also affects the charging of the capacitors.

5.5. Influence of the Internal Current Commutation Time of the DCCB

5.5.1. Behaviour of the DC Circuit-Breaker

The internal current commutation time (ICCT) is a key parameter of the DC circuit-breaker: the faster it is, the smaller the fault current. As seen in Figure 17, the maximum fault-current increase with the internal current commutation-time for Converter 1: the current rise is approximately constant between the blocking of the turn-off devices and the limitation of the fault current. The trend is different for Converter 2, the maximum fault-current is almost constant. Table 11 summarizes the main factors defining the operation of the DC circuit-breaker, for different internal current commutation times. It shows that the transient interruption voltage remains in an acceptable range despite a significant variation of the maximum fault current for Converter 1, because of the non-linearity of the MOV's electrical characteristic. Furthermore, the difference between the fault-current suppression time and the internal current commutation-time increases for Converter 1, because for a given di/dt a higher fault current takes longer to reach zero.

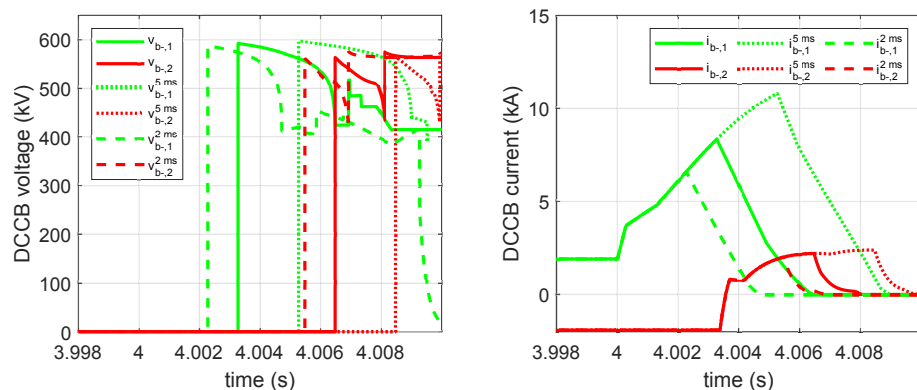


Figure 17. Current and voltage for the DC circuit-breakers of the negative poles of Converter 1 (green) and Converter 2 (red) with different internal current commutation times Δt_{ICCT} , dashed line for $\Delta t_{ICCT} = 2$ ms, solid line for $\Delta t_{ICCT} = 3$ ms and dotted line for $\Delta t_{ICCT} = 5$ ms.

Table 11. Electrical characteristics of the circuit-breakers' operation for different internal current commutation times (ICCTs).

Converter	Δt_{ICCT}	2 ms	3 ms	5 ms
1	Maximum fault current	6.60 kA	8.34 kA	10.8 kA
1	Fault current suppression time	4.70 ms	6.45 ms	8.99 ms
1	Transient interruption voltage	587 kV	592 kV	598 kV
2	Maximum fault current	2.01 kA	2.21 kA	2.39 kA
2	Fault current suppression time	6.86 ms	8.08 ms	9.89 ms
2	Transient interruption voltage	561 kV	563 kV	565 kV

5.5.2. Surge Current Integrals

Table 12 points out that surge current integrals are significantly affected by the internal current commutation-time: maximum surge current integral has been multiplied by 2.3 for

Converter 1 and by 2.1 for Converter 2, for an ICCT increasing from 3 ms to 5 ms. On the other hand, the maximum surge-current integral has been divided by 1.9 for Converter 1 and by 2.1 for Converter 2, for an ICCT dropping from 3 ms to 2 ms. As expected, the reduction of the internal current commutation-time of the DC circuit-breaker has a double positive impact on the surge-current integral. Therefore, this parameter is sensitive and should be properly estimated and managed.

Table 12. Surge current integral ($MA^2 \cdot s$) for D_2 with DC circuit-breakers for different internal current commutation times (ICCTs).

Δt_{ICCT}	2 ms	3 ms	5 ms
Converter 1	0.093	0.18	0.43
Converter 2	0.0046	0.0095	0.02

5.5.3. Overvoltages of the Cell Capacitors

The overvoltages of the capacitors can be problematic, especially in some cases lead to higher values than the ones previously observed. Figure 18 reveals that the maximum overvoltage appears to be contained but the modification of the ICCT changes the capacitors that are charged or not: with an ICCT of 5 ms, the capacitor of the upper arm of phase c is highly charged whereas it was almost constant with smaller ICCTs.

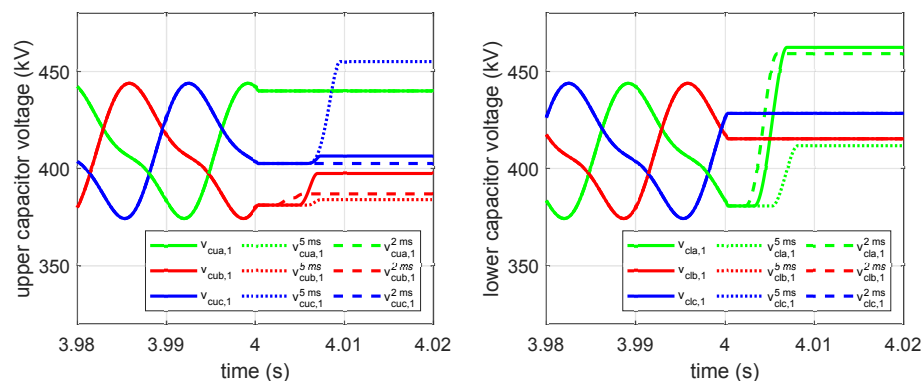


Figure 18. Capacitor voltages with different internal current-commutation times Δt_{ICCT} , dashed line for $\Delta t_{ICCT} = 2$ ms, solid line for $\Delta t_{ICCT} = 3$ ms and dotted line for $\Delta t_{ICCT} = 5$ ms.

6. Conclusions

The proposed simulation model offers many analyses of the behavior of an HVDC link under DC pole-to-pole fault conditions. Running under PLECS simulation software, it offers a reasonable computation time of about 10 min per simulation with a desktop computer. Meanwhile, it includes high-frequency response of the converters and the DC cables with a simple implementation, thus allowing a fault study of the whole system. A detection strategy has been implemented to properly compare different study cases.

The first comparison between AC circuit-breakers and DC circuit-breakers has revealed that the use DC circuit-breakers implies smaller design constraints for MMC's diodes. Surge current integrals, which are an important design factor, have been accurately calculated. The use of press-pack diodes in converter cells appears to be mandatory when using AC circuit-breakers in such HVDC links. On the other hand, fast fault-current suppression, brought by DC circuit-breakers, allows the use of devices with lower surge-current integrals. Having higher power densities, modules with IGBTs/IEGTs and integrated diodes, reverse-conducting devices, Bi-Mode Insulated Gate Transistors (BIGTs) or Bi-mode Gate Commutated Thyristor (BGCTs) may offer many features, such as higher cost-effectiveness or even higher reliability. Nevertheless, fault-limitation with DC circuit-breakers still leads to a charging of the cell capacitors above 1 p.u, which must also be considered in the design of the converter.

The influence of the DC circuit-breaker's characteristics has been studied, it can be concluded that the correct management of the internal current-commutation time is of paramount importance since it directly defines the maximum fault-current. From the point of view of the HVDC link, this paper has shown that the generic circuit-breaker proposed is effective enough to limit the effects of DC fault on the other converter stations: such conclusions are important when it comes to the design of multi-terminal HVDC links, where the best solution would be to isolate the faulty connection or the faulty converter station from the healthy ones.

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